Summary of PCS/PMA Logic for ACT/GMSLE Transceiver

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Objective

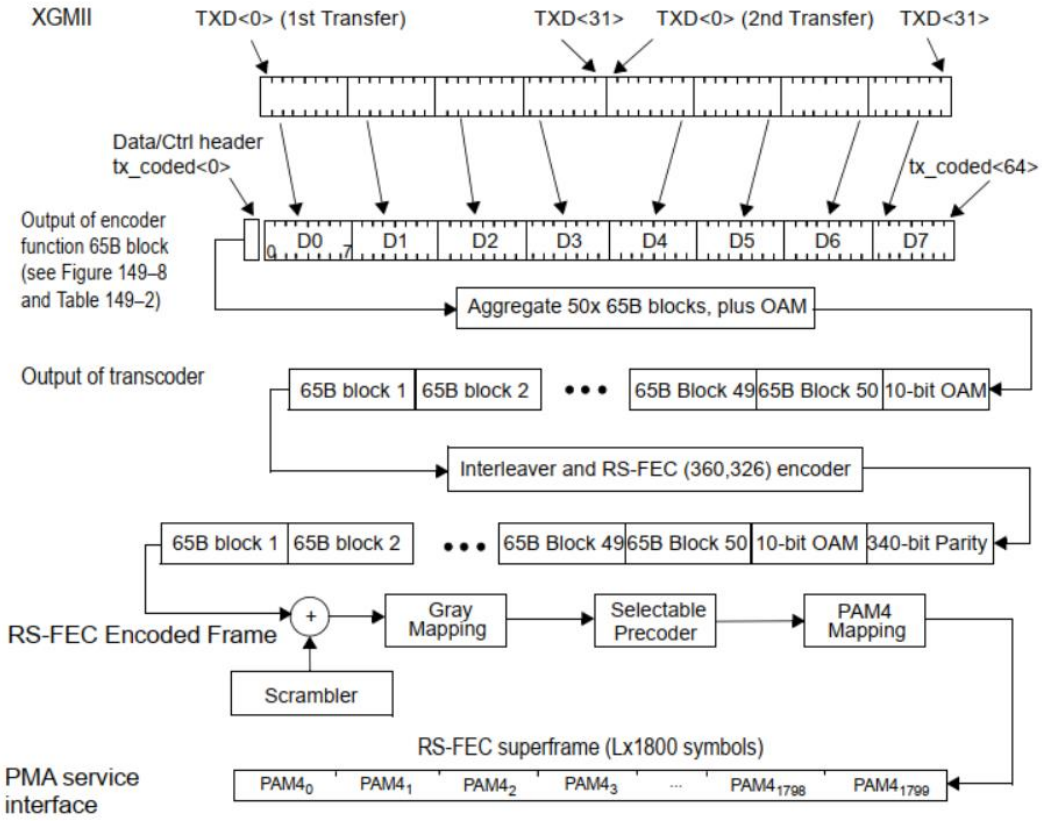
- Summarize points of consensus on PCS and PMA logic of ACT/GMSLE PHY
  - Make it easier to generate and understand text

- Taken some liberties to fill in missing details
  - Putting some details in place to get discussions going
  - Should not be controversial
  - Goal to get to consensus on details

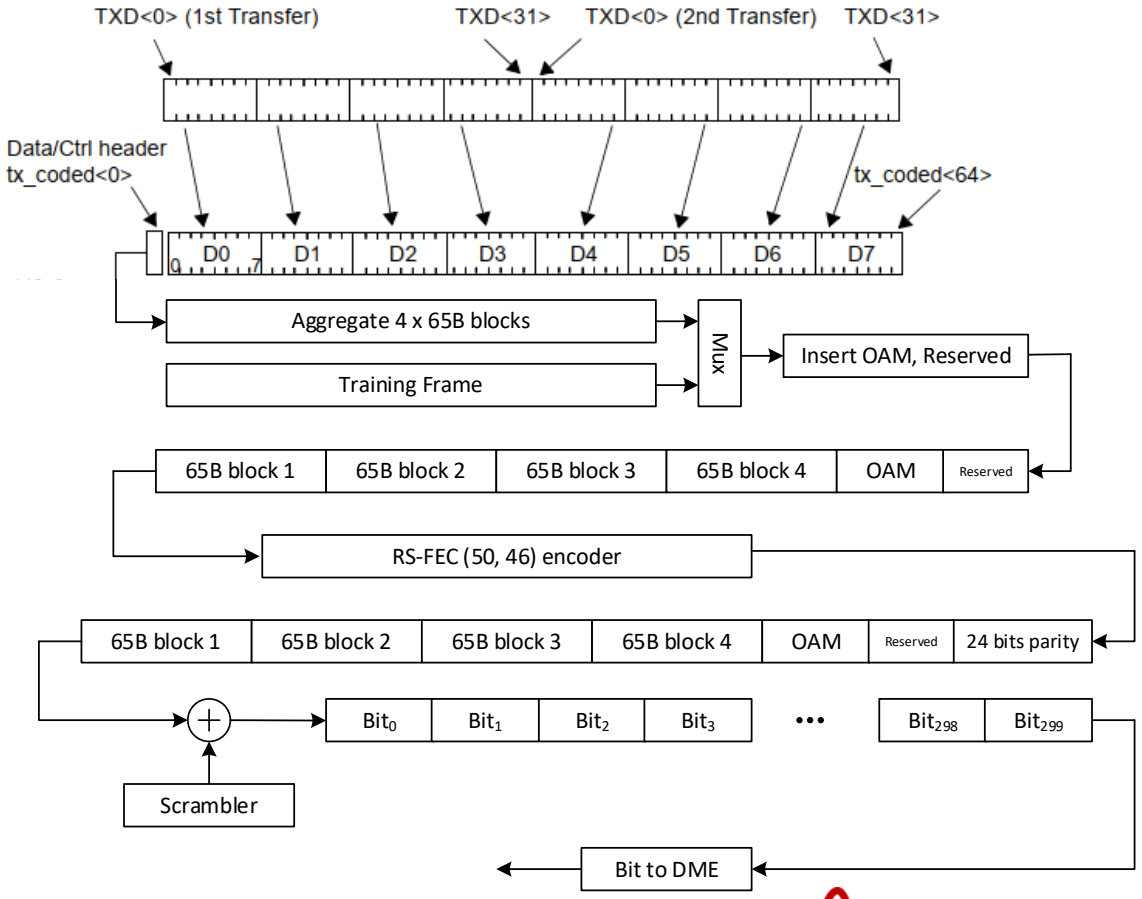
Transmit Path Overview

Downstream

- No change to clause 149



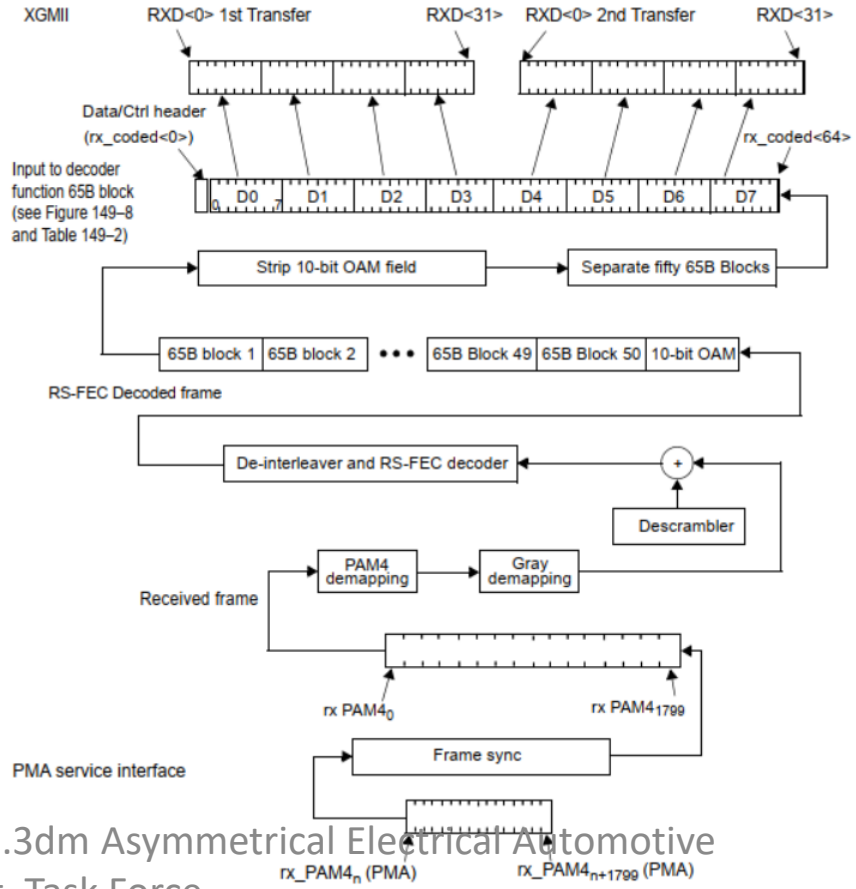
Upstream



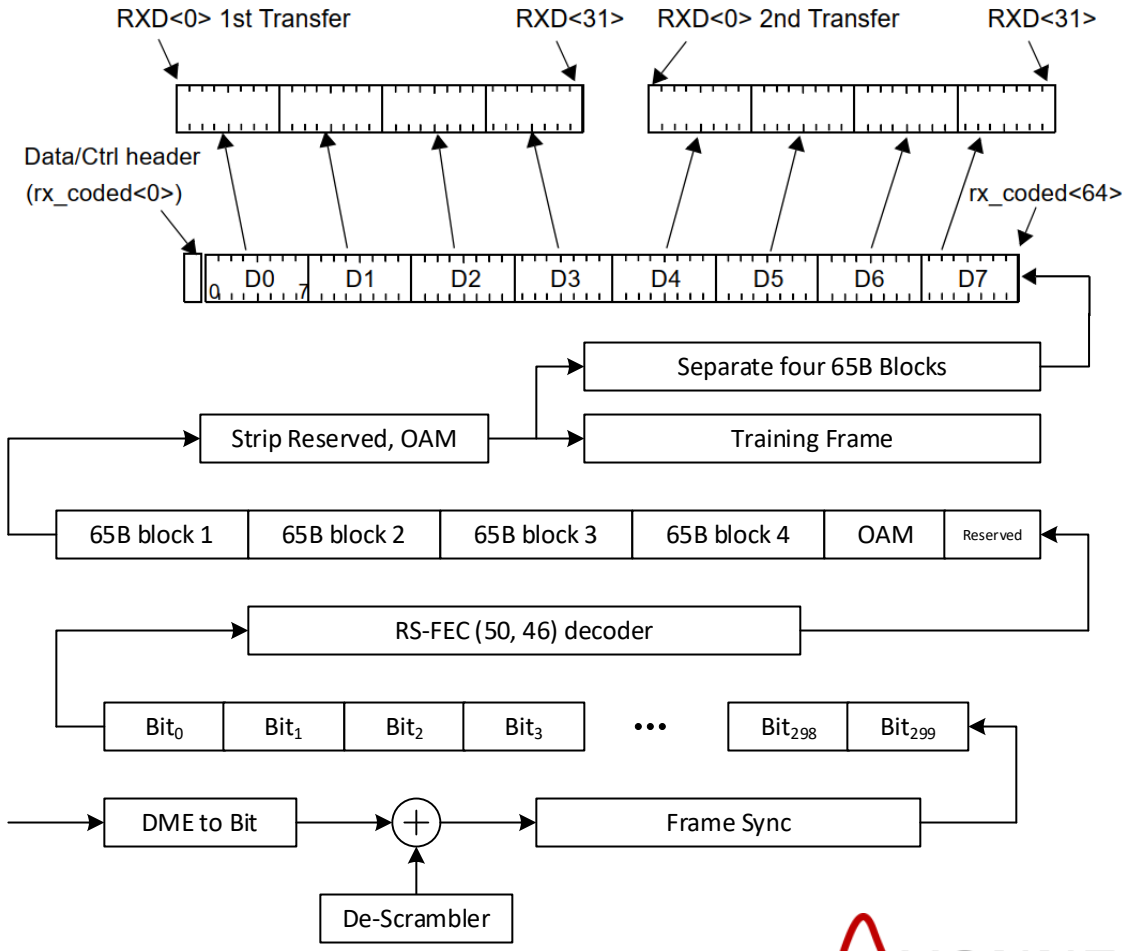
Receive Path Overview

Downstream

- No change to clause 149



Upstream



XGMII and Reconcilation Sublayer

Downstream

- No change to clause 46

Upstream

- No change to clause 46
- Clock speed is 1/100 of 10G.
  - Nominally 1.5625 MHz Clock
- Note
  - 100M MAC coupled to a reconciliation sublayer that supports start/terminate symbols and ordered set

64/65 Encoder/Decoder

Downstream

- No change to clause 149

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Upstream

- Transmit – no change to clause 149
- Receive – add a control code for training
- Decode C/D=1 Block = 0x00 as Local Fault

C/D								
1	Block	D0	D1	D2	D3	D4	D5	D6
1	0x00	D0	D1	D2	D3	D4	D5	D6

Block Aggregation

Downstream

- No change to clause 149
- 50 blocks of 64/65 + 10-bit OAM

Upstream

- 4 blocks of 64/65 + 10 bit OAM + 6 bits (all 1’s)

Reed Solomon

Downstream

- No change to clause 46
- RS(360, 326) GF(2^{10})
- g(x) = $\prod_{j=0}^{33}(x - \alpha^j)$
- $\alpha = x^{10} + x^3 + 1$
- no, 2x, 4x interleave – 10G
- no, 2x interleave – 5G
- no interleave – 2.5G

Upstream

- RS(50, 46) GF(2^6)
- g(x) = $\prod_{j=0}^{3}(x - \alpha^j)$
- $\alpha = x^6 + x + 1$
- no interleave

Scrambler/Descrambler

Downstream

- 802.3ch
  - Master: $g(x) = x^{33} + x^{13} + 1$
  - Slave: $g(x) = x^{33} + x^{20} + 1$

- 802.3dm
  - $g(x) = x^{33} + x^{20} + 1$
  - Independent of Master vs. Slave

Upstream

- $g(x) = x^{33} + x^{13} + 1$
- Independent of Master vs. Slave

Bit to Line Mapping

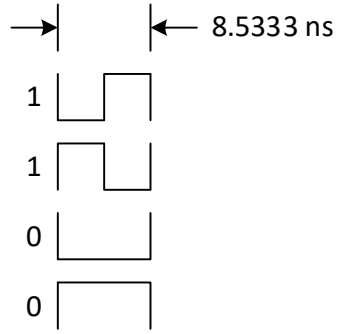
Downstream

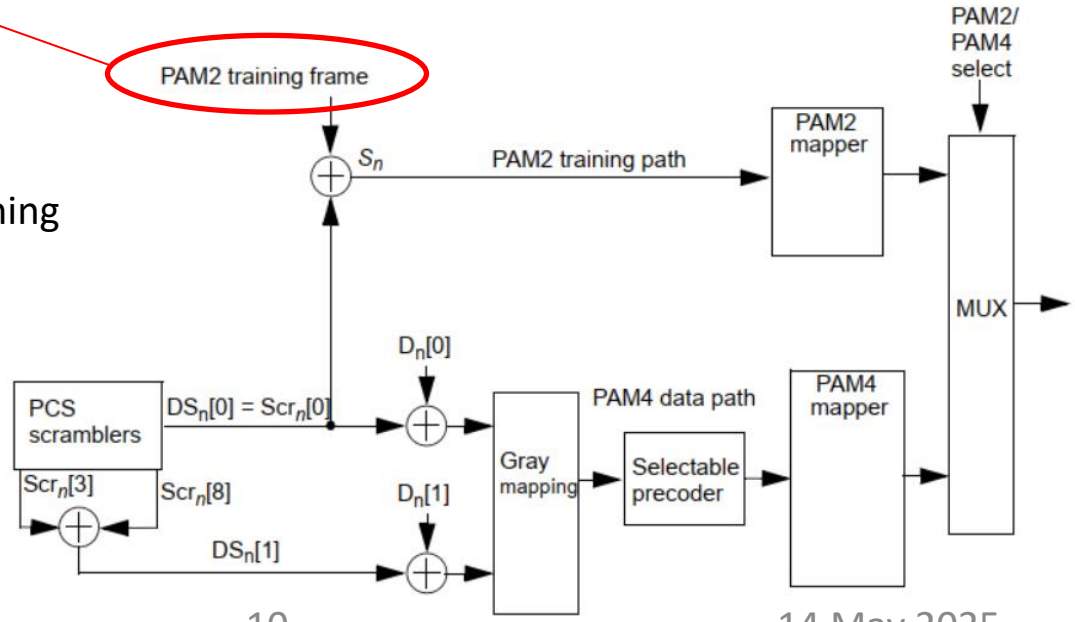
- 10G – no change from clause 149
  - 5.625 Gb/s PAM4 symbols
- 2.5/5G use training path for PAM2 PCS data
  - 5.625 Gb/s PAM2 – 5G
  - 2.8125 Gb/s PAM2 – 2.5G
  - Maintain same mapping as PAM2 training

    0 ➔ +1, 1 ➔ -1

Upstream

- Bit to DME





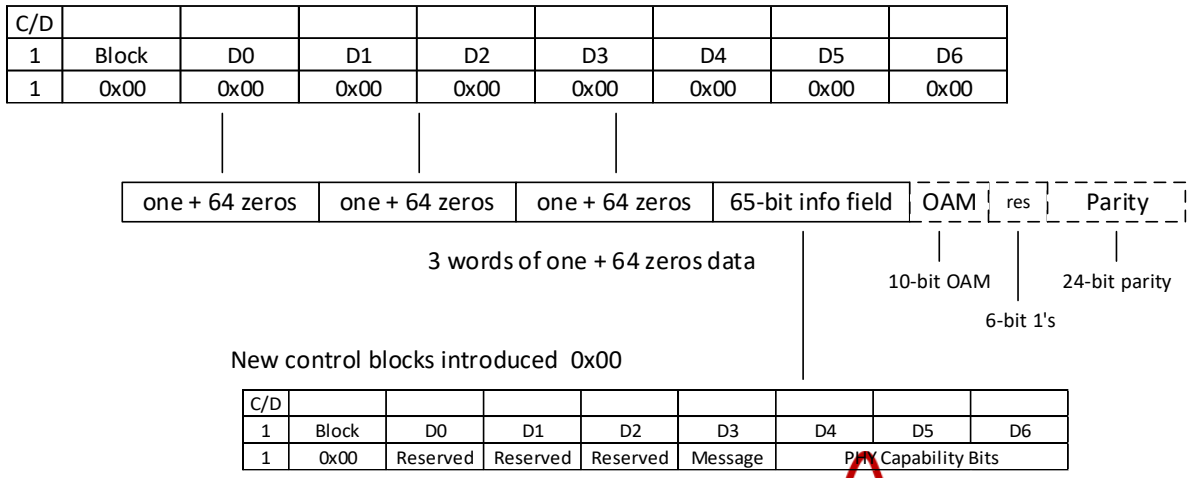
Training Frame

Downstream

- No change in logical framing to clause 149 except speed change
- 10G - No change 5.625 Gbaud
  - Training frame duration is 4 RS-Frame time
- 5G - 5.625 Gbaud
  - Was 2.8125 Gbaud in 802.3ch
  - Training frame duration is now 2 RS-Frame time
- 2.5G – 2.8125 Gbaud
  - Was 1.40625 Gbaud in 802.3ch
  - Training frame duration is now2 RS-Frame time

Upstream

- Baked into the data path
- Same DME signaling
- No countdown needed
  - Decode C/D=1 Block = 0x00 as training else normal data



Training Infofield

Downstream

- Message Field – Same as clause 149
- PHY Capability Bits
  - Eliminate – InterleaverDepth
  - Eliminate – PrecoderSel

Upstream

- Message Field – Same as clause 149
- Eliminate Partial Frame Count
- Simplification of PHY Control state diagram
  - No countdown needed

OAM

Downstream

- No change to clause 149

Upstream

- No change to clause 149
  - Pack 10-bit symbol onto RS frame

New Registers

- Device 1 – Add 802.3dm capabilities (total 6 capabilities)
  - Ability register
  - Control register
- Device 7 - Add 802.3dm capabilities
  - Auto-Negotiation Technology Ability Field Assignments (6 new bits)
  - Need to determine priority resolution
    - Asymmetrical pairings now

Reuse Existing Registers

- 1.2309 – PMA Control
- 1.2310 – PMA Status
- 1.2311 – Training
- 1.2312 – Link Partner Training
- 1.2313 – Testmode Control – (may need modification??)
- 1.2314 – SNR
- 1.2315 – Minimum SNR
- 1.2316 – User defined Register
- 1.2317 – Link Partner User defined Register

Reuse Existing Registers

- 3.2308 – OAM Transmit
- 3.2309 to 3.2312 – OAM Message
- 3.2313 – OAM Receive
- 3.2301 to 3.2317 – Link Partner OAM Message
- 3.2318 to 3.2319 – OAM Status Message
- 3.2320 to 3.2321 – Link Partner OAM Status Message

Reuse Existing Registers

- 3.2322 – PCS control except bit 14 loopback does not apply
- 3.2323 – PCS Status
  - bits 8 to 11 may or may not apply
- 3.2324 – PCS Status 2

THANK YOU