Crystal-less operation of a TDD PHY

IEEE 802.3dm

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Background & Motivation

- It is highly desirable to have crystal-less implementation of PHYs in sensor modules to achieve relative lower cost.
- Some participants have expressed skepticism related to crystal-less operation with TDD PHYs
- This contribution describes a thoughtfully devised experiment to demonstrate the technical feasibility of such operation
- Actual TDD based (ASA-ML) silicon is used for the experiment in this contribution

Background contd..

- TDD PHY specifications proposed in TF facilitates crystal-less operation as follows
  - Precise duplexing beat of ~100kHz
  - Refresh/Resync header for clock/data alignment
  - CDR/Loop Timing can also be employed depending on the implementation
  - Generic SERDES CDR is expected to be sufficient
- If one simply presents a setup and states it “works”, it would be hard to establish the details
- We used the setup described in the next slide to demonstrate feasibility

Setup for the feasibility demonstration

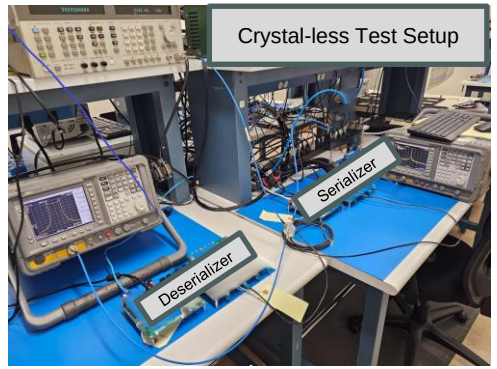
- A key aspect of Crystal-less Serializers is the jitter/stability of internal oscillator
  - A low-cost reference can be an on-die oscillator that lacks precision/stability of crystal
  - Its temperature drift can be mostly calibrated out and center frequency can be tuned
  - Accounting for residual noise and frequency offsets/drifts is then implementation specific

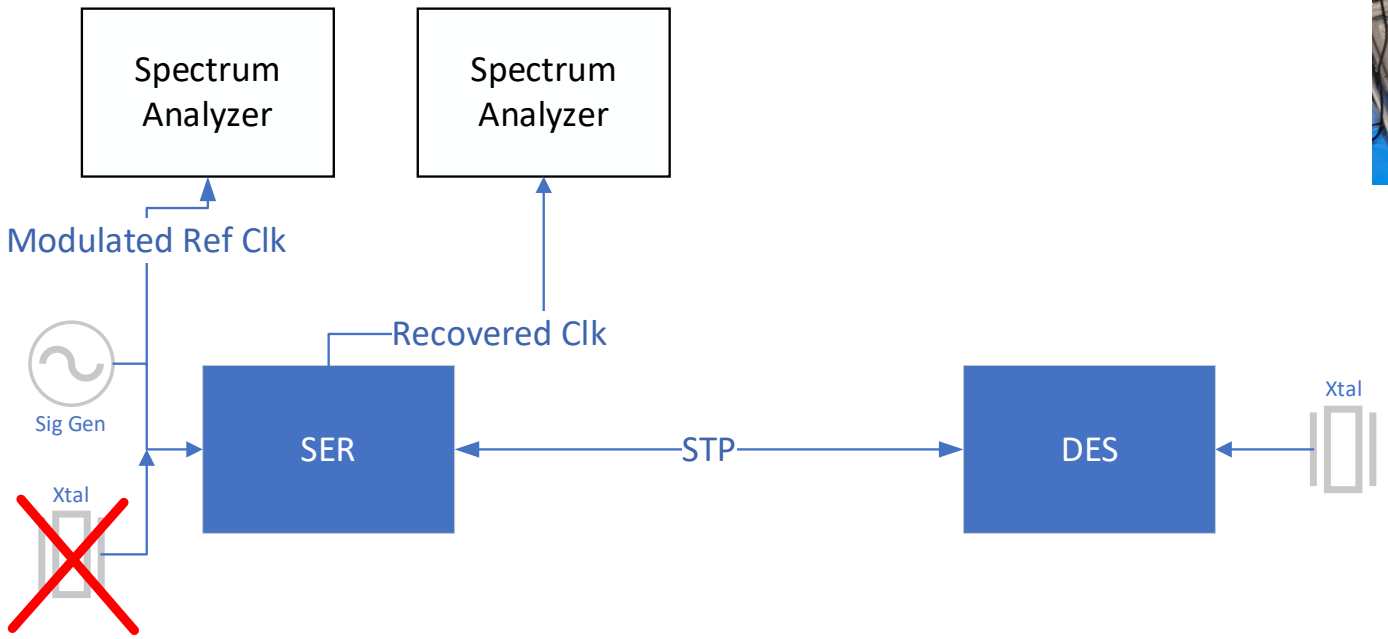
- To mimic pathological on-die oscillator, we used a non-ideal external clock
  - Used + or -100ppm static offset
  - Modulated with an additional ± ppm at high rate to exceed expected post calibrated drift

- Observed (a) ext clk, (b) recovered clock and (c) BER
  - External reference clock mimicking on-die oscillator should show spreading
  - Recovered clock used for SER TX should be a single tone in a successful experiment
  - Received BER should not be different than when using a crystal

Test Setup

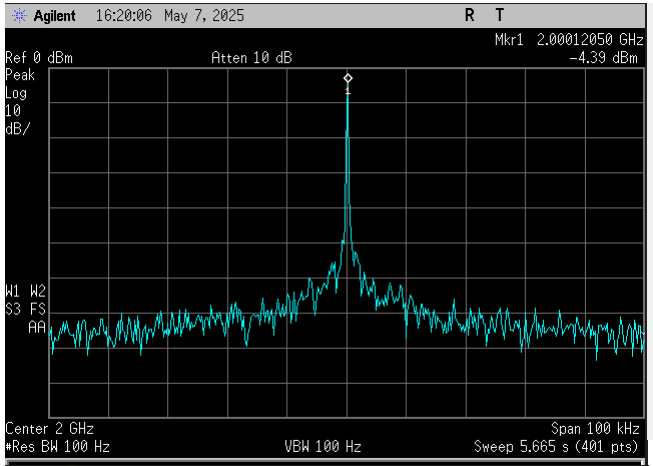
- Mimicking of a pathological internal oscillator
  - 99.99 MHz external clock (static -100ppm)
    - Force large ±150ppm modulated offsets
    - Force 300ppm excursions in 5 seconds
- ASA based TDD PHY in SG3/SG1 (8GSps↓ 2GSps↑)
- ASA based TDD PHY in SG5/SG1 (PAM4 8GSps↓ 2GSps↑)
- 5m STP

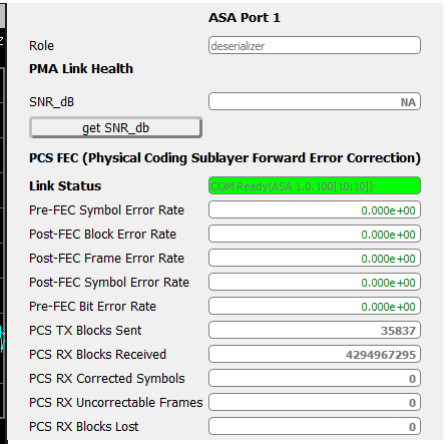


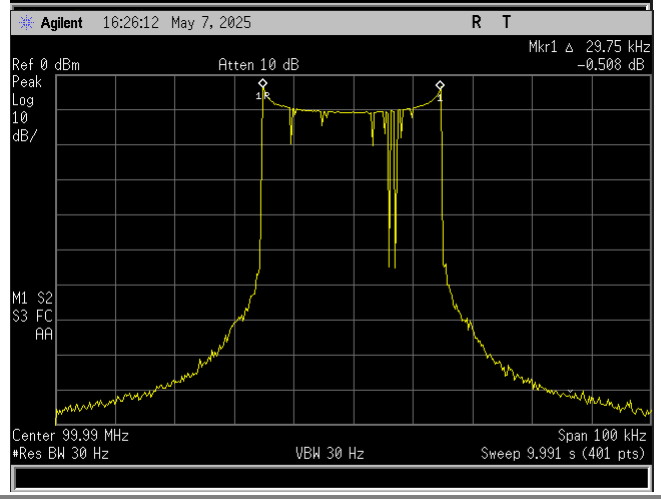


Results

- ASA SG5/SG1
  - Serializer CDR lock
  - Deserializer error free







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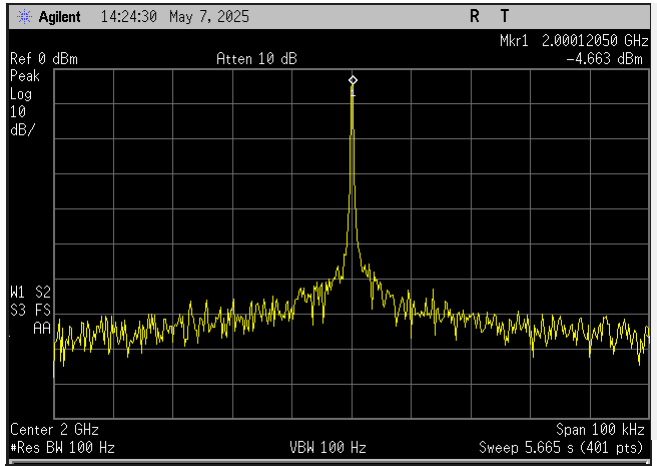

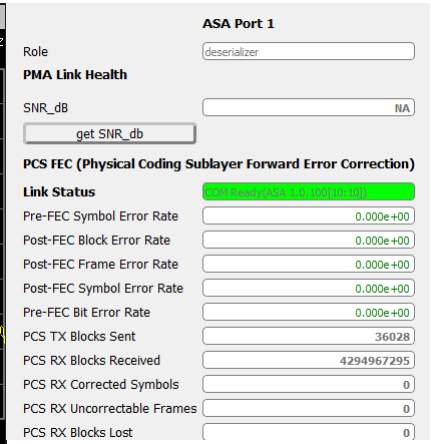

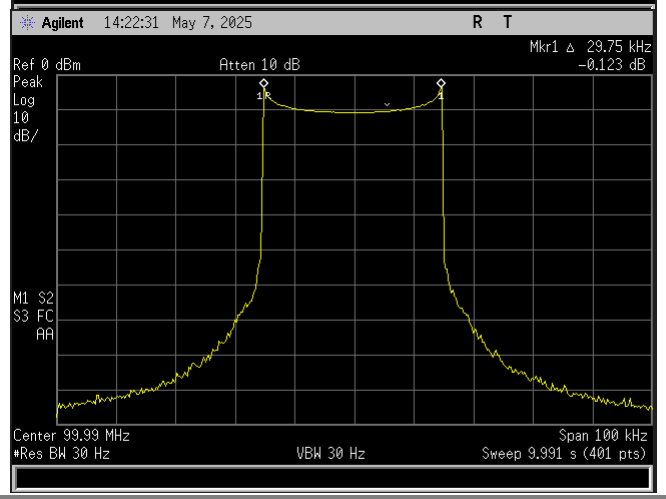

Summary

- The contribution describes the setup used for the experiment to establish feasibility of crystal-less TDD Serializers
  - Feedback wrt extent of static and modulated frequency offsets is welcome
- Provided silicon measurements for the described experiment
  - Error free operation in ASA SG3/SG1 with CDR lock as expected
  - Error free operation in ASA SG5(PAM4)/SG1 with CDR lock as expected
- This experiment demonstrates that crystal-less TDD Serializer is easily achievable

Thank You!