ACT and TDD Comparison

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Contribution to 802.3dm Task Force
30 July 2025

Introduction

This is a continuation of May – New Orleans Interim comparison done by TJ Houck and Jay Cordaro.

Objective #1: Summarize presentations that have been given thus far and major areas of difference between ACT and TDD that impact relative cost and future system development

Objective #2: Group past presentations into appropriate section and provide information on each topic of importance

Previous Comparison Presentation: May Interim

IEEE 802.3dm PHY evolution Comparative Analysis for GMSLE, ACT, and TDD approaches

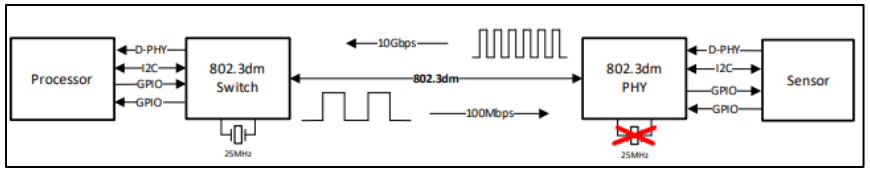
March Interim – Jay Cordaro - GMSLE FDD PHY Simulation Results and PHY Complexity

Comparison Table

	ACT – Proposal	TDD – Proposal
Crystal-less	**Proven working solution for ACT** SERDES also has a proven working solution in mass production GMSLE Baseline Proposal for IEEE 802.3dm Lo_3dm_01_050125.pdf | Razavi_3dm_01a_May_01_2025.pdf	**Theorized** – several subjects left open still Ng_3dm_01_05122025.pdf
EMC – Radar Pulse	**Proven** ACT silicon – **Passed 600V/m** – **UNSHEILDED** Equal or **Surpasses** SERDES and Ethernet on the market today jonsson_3dm_01_07_15_24.pdf | GMSLE FDD PHY Simulation Results and PHY Complexity wu_3dm_01_072925.pdf	**Did not test** Radar pulse at 300V/m or 600V/m Zerna_3dm_01_250729.pdf | Dalmia_Ng_EMI_COAX_3dm_01_04172025.pdf
Power consumption	**Best** Power performance due to **low complexity** Comparative Analysis for GMSLE/ACT, and TDD sedarat_3dm_02_202503.pdf - contains 8 presentation links	**Equal** w/ power control or **Higher** w/ no power control >3x the power of ACT w/ no power control **Requires power reduction circuitry that will cause die size increase to achieve near equal power to ACT** Chini_3dm_02b_0325.pdf
Size and complexity	**Smallest die size** shown in several presentations due to **low complexity** Houck_3dm_01_0121_5.pdf | jonsson_3dm_02_06_26_25.pdf	**Larger die size** due to higher speed rates and **TDD complexity** Chini_3dm_02b_0325.pdf
Longer Cable Length	**Capable of 20-30meters** with standard coax Propagation Delay = **160nsecs** – limited by insertion loss Link Propagation Delay in IEEE 802.3dm: System Implications and Trade offs	Capable of **No** more than **15meters – collisions possible** jonsson_3dm_01_06_26_25.pdf Propagation Delay proposed = **84nsec** gorshe_3dm_01_250710.pdf
Future for 25Gbps	**Less complexity** solution for high-speed, full duplex payload delivery PAR Scope and Physical Layer Rates between 10 Gbps and 25 Gbps	**Most complex path to 25Gbps** – requires higher PHY rates, strict timing, and burst synchronization PAR Scope and Physical Layer Rates between 10 Gbps and 25 Gbps
Interoperability	PHY vendors can **leverage 802.3ch PHYs**	TDD – **ASA with changes and large compatibility issues** IEEE 802.3dm PHY evolution Comparative Analysis for GMSLE, ACT, and TDD approaches
Image and Switch Integration	**Lowest complexity**	**More complex**
PoC complexity	**1 inductor** GMSLE FDD PHY Simulation Results and PHY Complexity From Concept to Circuit: Designing Effective PoC Filters	**2 inductors** – no 1 inductor solutions with 15m w/ 4inlines Chini_Tazebay_3dm_01a_0924.pdf jingcong_dm_2024Sep_v2.pdf | jonsson_3dm_02_06_26_25.pdf

Crystal-less Summary

- Crystal-less operation was passed as a motion to be an 802.3dm **objective**
- Crystal-less operation is **achievable** and **proven** in ACT
- TDD's time-duplex nature makes this significantly more challenging, requiring higher timing margin or oscillator solutions.



Houck_Ragnar_Fuller_3dm_01_0917.pdf

- **TDD Limitations**
  - Requires bidirectional coordination – receiver **can't receive clock reference during TX phase**
  - Going from 100KHz to 6GHz requires a **multiplier** of **60,000**
  - Typically requires a **local crystal** or **high stability XO** to maintain link fidelity between TX/RX cycles

https://ieee802.org/3/dm/public/0924/Houck_Ragnar_Fuller_3dm_01_0917.pdf

- **ACT Advantages**
  - **x1,250 easier clock recovery** than TDD going from 117MHz to 5.625GHz is only a multiplier of 48
  - Concurrent transmission allows for **continuous timing updates** (no guard bands needed for training)
  - Receiver clock can be **continuously** steered

EMC – Radar Pulse

Radar Pulse test is one of the most difficult Radiated Immunity tests to pass in automotive.

Band	Frequency Range (MHz)	Level 1 (V/m)	Level 2 (V/m)	Modulation
4	400 - 800	50	100	CW, AM 80% Pulsed PRR= 18 Hz, PD= 28 msec (1)
5	800 - 2000	50	70	CW, Pulsed PRR= 217 Hz, PD=0.57 msec
6	1200 - 1400	n/a	300 600 (2)	Pulsed PRR= 300 Hz, PD = 3 usec, (3) with only 50 pulses output every 1 sec. (1,2)
7	2700 – 3100	n/a	300 600 (2)	

1. Pulse Modulation limited to 400 – 470 MHz
2. 600 V/m requirements are only applicable to selected components associated with supplemental restraints system including frontal crash sensors. Contact FMC EMC department for specific applicability
3. Pulse duration (PD) shall be extended to 6 usec when testing using the reverberation (mode tuned) method. See 11.4.2.2 for additional detail.

https://www.elect-spec.com/download/EMC_CS_2009rev1.pdf

TDD Limitations

- TDD systems must precisely align their TX/RX windows every 8.667us – A 600V/m radar pulse **overlapping** this turnaround window can **disrupt timing calibration** and analog front end biasing
- TDD is vulnerable during RX/TX transitions – especially if a high-energy radar pulse hits
  - Just before or during RX startup
  - While RX bias is not yet stabilized
  - Weaker FEC than ACT

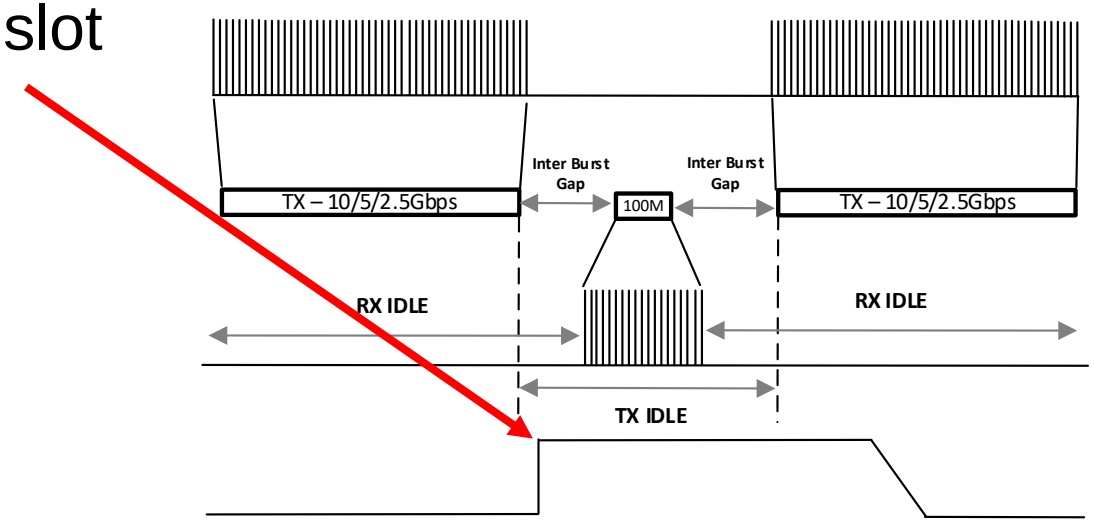
ACT Advantages

- **Immediate** absorption and correction of noise
- No **dropouts** or **retraining**
- **Far more** robust EMC behavior under 600V/m radar pulses
- **No echo cancellation** is required to achieve passing results

EMC – Radar Pulse

Pulses are 1-3us wide ~10-30% of the TDD slot

- If a pulse overlaps the mode switching it can
  - Disrupt bias stabilization
  - Break RX slicer threshold lock
  - Invalidate adaptive equalizer state
  - Cause TX/RX misalignment



	ACT	TDD
RX stability during pulse	**Continuous and adapts**	**Interrupted**
Impact of Pulse on TX/RX	**No switching** between TX/RX	**High Risk**
EMC recovery	**Real-time** resilience	**Requires resync**
Suitability for 600V/m	**Robust**	**Weak**

Low Power Summary

- TDD claims lower average power due to TX/RX low duty cycle
- However practical PHY constraints (CDR, AGC, PLL, state retention) require always-on analog paths, limiting power savings

- ACT achieves similar or **better** power with less design risk complexity and overhead

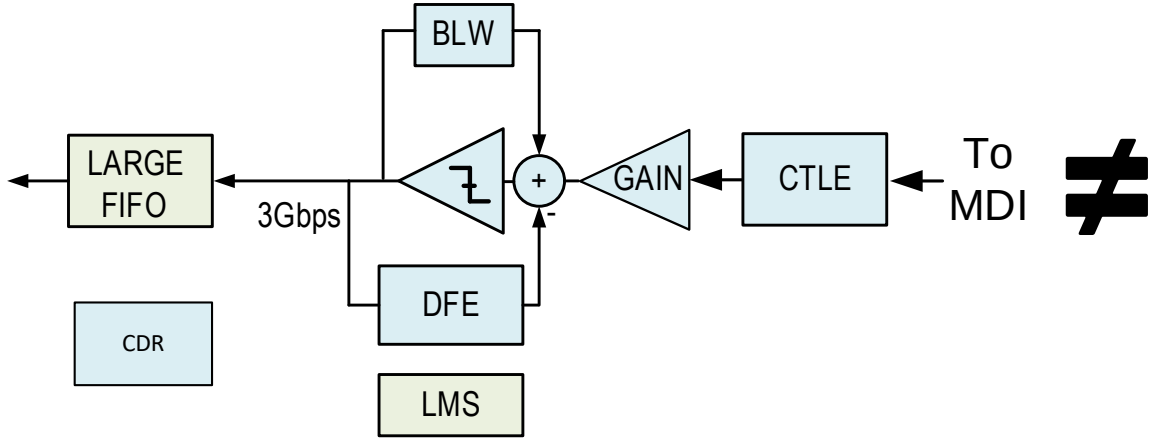
	ACT	TDD
Power Savings Mechanisms	**Not needed** - Continuous transmission	Analog bias throttling, retention logic, digital clock gating
Analog Power Gating	**Not required** – Continuous	**Not fully power down** – CDR, PLLs. AGC, and DFE must remain biased
Retention Overhead	None – does **NOT** need to shutdown	**+10-15% Increase** digital power for FSM + Analog state retention
Die Area Impact	**Baseline** (1.00x)	**+25-35% Increase** due to retention, isolated cells, FSMs, power gating
Relative Design Complexity	**Low** – No special power saving modes needed	**High** – due to above complexity for power savings

802.3dm Sensor-side complexity: ACT vs TDD

	ACT	TDD
Camera Downstream highspeed TX Complexity	**Least complex**	More complex ▪ TDD
Camera Upstream lowspeed RX Complexity	▪ Less Complex	Much more complex ▪ TDD ▪ BLW Comp ▪ DFE EQ ▪ LMS ▪ FEC ▪ FIFO
Camera Power Consumption	▪ **Lowest**	▪ In same geometry, higher power consumption ▪ Clock gating can lower power consumption but raises complexity
Camera LS RX FEC	n=50, k=46, m=6, t=2	~~n=130, k=122, m=8, t=4~~ n=130, k=124, m=8, t=3 no longer same code US/DS
Camera LS RX FEC decoder area complexity^	Baseline ▪ 1.0x Least Complex^	▪ 215%-540% additional complexity, depending on implementation and either fixed n and fixed r=n-k or reuse of (Chien) DS IP at US ▪ Chien Latency processing > 2x, but faster fill rate ~ draw ▪ Low latency combinatorial decoder possible but still much more complex than n=50, k=46, m=6 t=2 combinatorial decoder
Upstream burst protection	51.2ns	~~▪ 10.6ns~~ ▪ 8ns much less than ACT
Crystal-less Camera Serializer	Simple.	Possible, but more complex
Upstream latency (including FEC)	~8µs	~9.6µs (est., based on TDD presentation)
Summary	**Lowest Complexity** for 3MP 2.5Gbps and 8Mp 5Gbps cameras	▪ **Highest complexity.** ▪ **Raises cost, power for 3MP 2.5Gbps and 8MP 5Gbps cameras.** ▪ **XTAL-less more complex.** ▪ **Lower burst protection length >6x**

Upstream Receiver Comparison TDD vs. ACT

TDD Upstream Receiver



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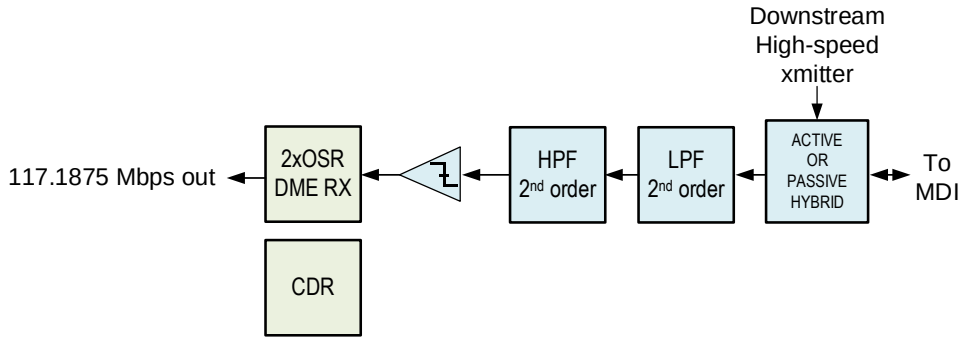
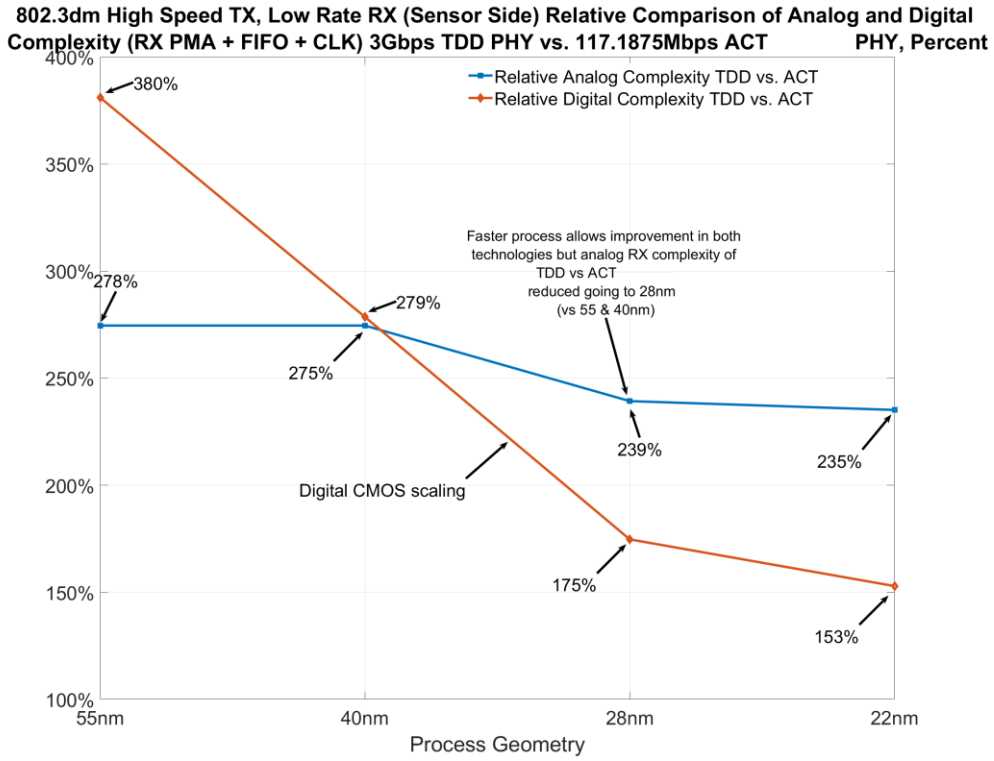
ACT Upstream Receiver

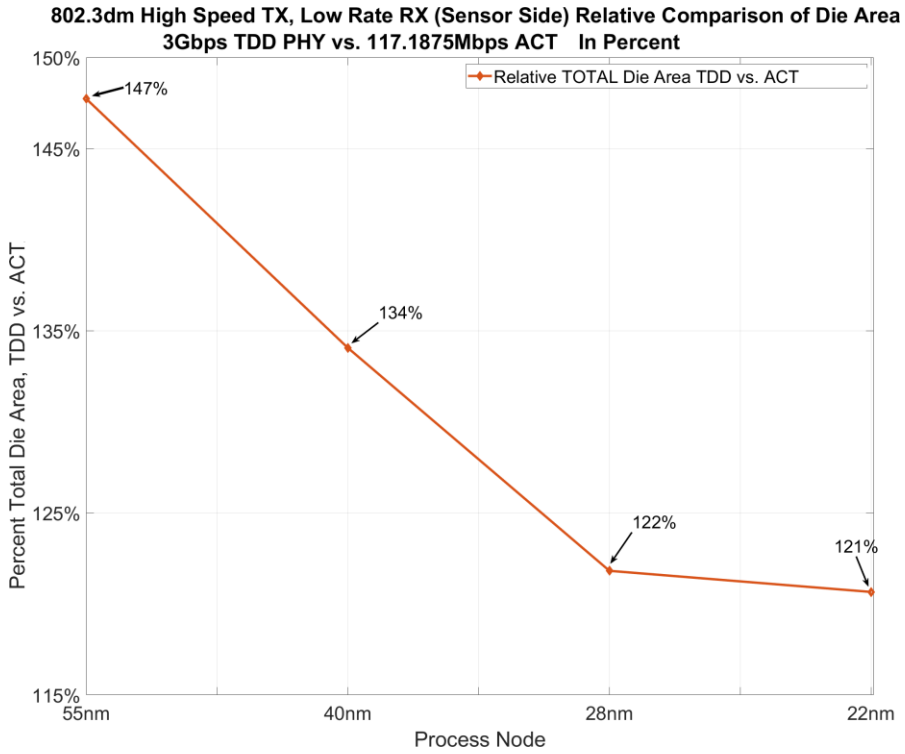


- The two PHYs largely have similar functional blocks
  - ESD protection, MAC interface, PHY Control State Machine, GPIO, temp monitors, etc.
- The difference is in the duplexing, partial frequency overlap duplexing or time division duplexing of the channel
  - PLL, PMA RX (major – DFE, LMS, FIFO size, power gating, as well as padring, FEC, CDR/PLL, baseline wander correction, clock tree)
- Let's evaluate the complexity of sensor PHY (high speed transmit, low speed receive)
  - Analog-based (no ADC) implementation for both
  - Consider the relative complexity of the PMA RX and associated blocks
  - Consider the relative complexity of the entire die
    - For entire die analysis, consider everything (ESD, padring, test, calibration)

} Evaluate both RX and total in same geometries

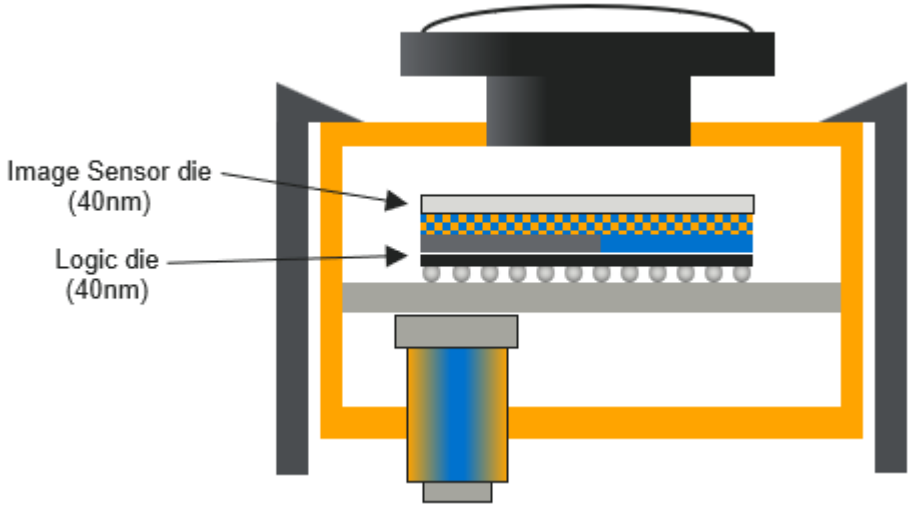
Sensor-side PHY Receive Portion and Overall Relative Area





- More detailed analysis than previous at 55nm and 28nm of all relevant blocks and entire die including padring
  - 40nm and 22nm extrapolated from 55nm and 28nm nodes, respectively
- 28nm and 22nm allow a more CMOS approach which helps reduce die area versus CML in larger nodes.
  - Helps reduce the complexity of BOTH PHYs, but comparatively helps TDD more since its receiver is much more complex.
- Sensor CMOS dies will stay at 40nm, 28nm and 22nm for the near future
- **Additional relative complexity of RX and total die for TDD vs ACT in 40nm, 28nm, 22nm is significant**

PHY integration in the Imager



Compared to TDD, ACT offers:

- Smallest size
- Lower complexity (no need for buffers and synchronization mechanism)
- Better suitability for older process nodes
- Better suited for Crystal-less operation

https://www.ieee802.org/3/dm/public/0924/jonsson_razavi_3dm_01_09_15_24.pdf
https://www.ieee802.org/3/dm/public/1124/Houck_Fuller_3dm_03_1111.pdf

Unlike TDD's 3Gbps receiver, ACT's 100Mbps receiver is much less complex.
ACT can be implemented in process nodes typically used for image sensors (40nm), while TDD implementation might require a more aggressive process node.

PHY integration in the Switch

Product considerations: To ensure flexibility and maximize utilization of all switch ports, it is highly desirable that **each Multi-Gig PHY port** supports either **asymmetrical 802.3dm** (camera link) or a **symmetric 802.3ch** connection.

Multi-mode port: 802.3ch + 802.3dm
based on ACT

Ethernet Switch

Updates to make 802.3ch PHY multi-mode:
- Add 100Mbps transmitter

802.3ch PHY
100M Tx

Multi-mode port: 802.3ch + 802.3dm
based on TDD

Ethernet Switch

Updates to make 802.3ch PHY multi-mode:
- Add 3Gbps PAM2 transmit support
- Add 3Gbps PAM2 receive support
- Add 6Gbps PAM2 receive support
- Add 12Gbps PAM4 receive support
- Add TDD synchronization mechanism
- Add TDD buffers for upstream and downstream

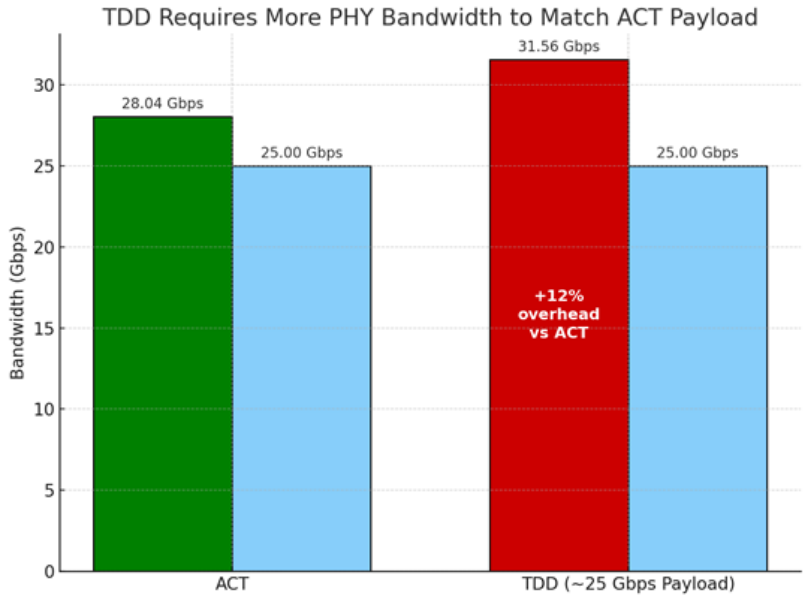
802.3ch PHY

Interoperability between TDD and ASA

	TDD – Proposal #1	TDD – Proposal #2	TDD – Proposal #3	ASA 2.0 (MLE)	ASA 2.1 (MLE)
Released	Nov 2024	Jan 2025	May 2025	May 2024	Feb 2025
Baud rate	3.125 Gsps / 6.25 Gsps	3.0 Gsps / 6.0 Gsps	3.0 Gsps / 6.0 Gsps	SG1- SG5 2/4/6/8 Gsps	SG1- SG5 2/4/6/8 Gsps
Cycle timing and encoding	Fixed – 8.96usec – 896ns 64b65 and 80b/81b	Fixed – 9.6usec – 933ns 64b65b	Fixed – 9.6usec – 933ns 64b65b	2.5us – 26.832us (SG driven) 64b65b	2.5us – 26.832us (SG driven) 64b65b
FEC	8bit – RS – 3 FEC types 9bit – RS – 3 FEC types	1 FEC for all speeds 8bit – RS – 130,122	2 FECs needed UL/DL 8bit – RS – 130,122 (UL) OAM – 1bit 8bit – RS – 130,124 (DL) OAM – 17bit	240,214	240,214
Link start up procedure	Fixed time slot w/ predefined burst	Fixed time slot w/ predefined burst	Fixed time slot w/ predefined burst	Multi-phase dynamic training with OAM message exchanges and PTB clock alignment	Multi-phase dynamic training with OAM message exchanges and PTB clock alignment
Burst timing and switch logic	Fixed – PTB?	Fixed time slot w/ predefined burst	Fixed time slot w/ predefined burst	Deterministic – PTB based 6844 – PTB tics Fixed Quiet gap Anchored to StartTDD	More robust startup Variable w/ (628-6708) PTB tics Refined for shorter Upstream Same – better startup phases
OAM	Not defined	Not defined	Not defined	Occurs during startup and dynamical for updates	Occurs during startup and dynamical for updates
Clock leader and PTB	Not defined	Not defined	Not defined	Foundation for synchronization and timing accuracy	Foundation for synchronization and timing accuracy
ASEP	Needs DLL extensions, config. space, and stream sync procedures	Needs DLL extensions, config. space, and stream sync procedures	Needs DLL extensions, config. space, and stream sync procedures	Supports	Supports

Future for 25Gbps

- TDD requires **significantly** more PHY bandwidth than ACT to deliver the same payload
- Inefficiency compounds with speed
  - As speed increases – IBGs, burst turnaround, and resync framing consume proportional larger data
- ACT uses **continuous** full-duplex streaming avoiding:
  - Resync bursts and Guard bands
- Higher PHY speed for TDD = **MORE die area and MORE power**
- TDD breaks down above 10Gbps – “the inefficiencies scale faster than data”



ACT calculation: FEC 90.56% x 64/65b = 89.15% x 25Gbps = 28.04Gbps
TDD calculation: 8.2745µs/9.6µs = 0.862 x 64/65b x FEC 93.86% = 31.56Gbps

Full cycle = 9.6µs
FWD transmit = 8.667µs
IBG = 106.66ns x 2 = 213.33ns
Resync (doubled) = 4480b @ 25Gbps = 179.2ns Usable transmit time = **8.2745µs**

ACT Line rate for 25Gbps: 28.04Gbps
TDD Line rate for 25Gbps: 31.56Gbps – 12% MORE than ACT

Longer Cable Length Summary

- Insertion Loss must drive link length requirement **NOT** delay.
  - This will limit markets outside of automotive – Trucking, bussing, aero, industrial, robotics, agricultural, biomedical, etc.

- This is an issue on 802.3ch which prevents customers from achieving longer cable length and will become problematic for the standard if they want cable lengths further than 15meters.

802.3ch Link Delay = 94ns

149.7.1.6 Maximum link delay

The propagation delay of a link segment shall not exceed 94 ns at all frequencies between 2 MHz and F_{max} MHz.

Current TDD proposal does not even exceed 802.3ch = 84ns

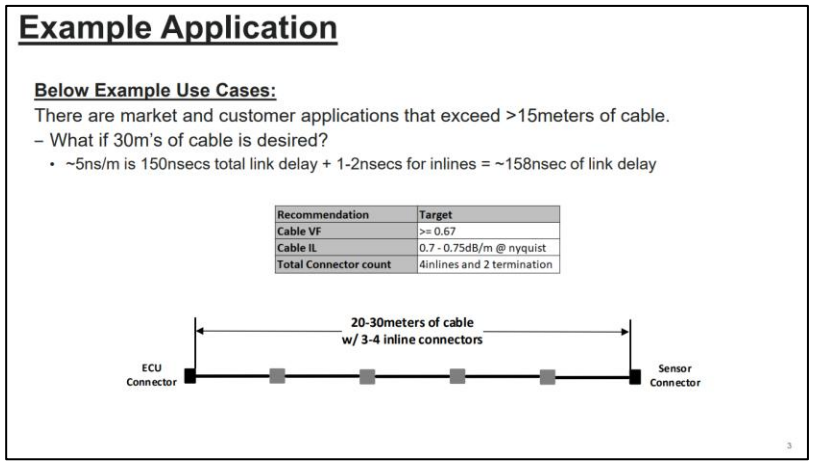
recommend the value of no more than 84ns for coaxial cable, which already a compromise in that it adds >7ns of margin to the calculated value for 15m

Longer Cable Length Summary

- Key statement was **not** included on past presentation favoring <15meter cabling are the PAR stakeholders

> **5.6 Stakeholders for the Standard:** End-users, automotive Original Equipment Manufacturers (car makers) and Tier x automotive suppliers, system integrators, and providers of systems and components (e.g., cameras, sensors, actuators, artificial intelligence (AI) processors, instruments, controllers, network infrastructure, user interfaces, and servers) for automotive and other transportation, building and industrial automation, and biomedical applications.

- Automotive cable presentations have shown further length is **achievable** with **standard AGED CX44**
  https://ieee802.org/3/dm/public/adhoc/062625/Koeppendoerfer_3dm_coax_performanve_01_06262025.pdf



802.3dm May Interim Link Delay Presentation

Cable (CX44) Insertion Loss at 2.8GHz ~0.8dB/m (above presentation)

Proposed IL @2.8GHz = -23.08dB
boyer_sharma-3dm_xx_05-14-25_3.pdf

Total **Achievable Length** = -23.08dB/-0.8dB/m = **28.9meters**

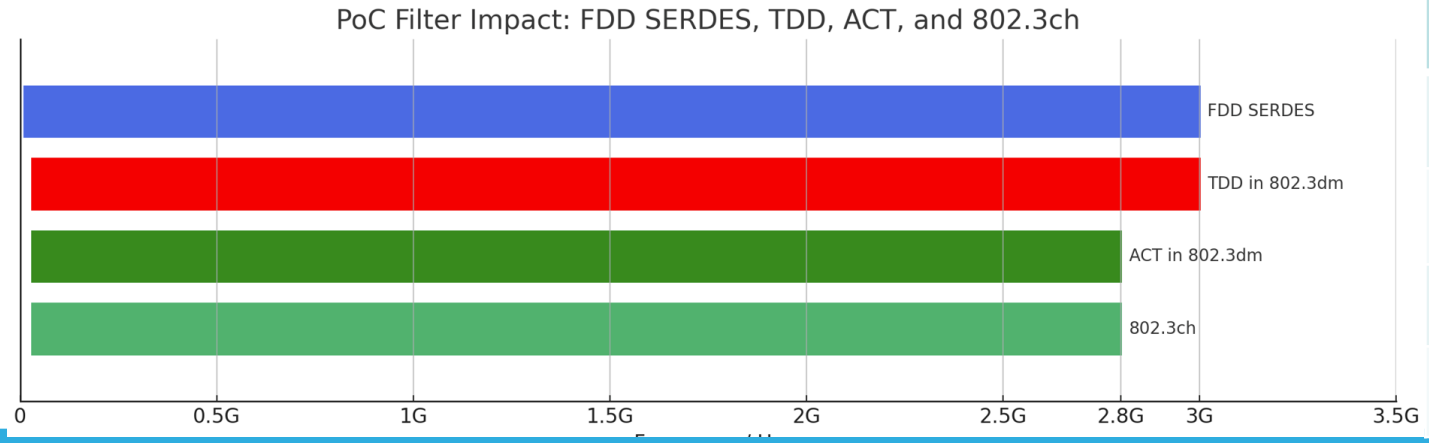
Proposed propagation delay for ACT: **160nsecs**
Total Link delay 5ns x 28.9meters = 144ns (cable)+ 8ns (connectors) = **152ns**

PoC Complexity

- **Current SERDES** solutions have a **1 inductor** and ACT shifted the upper and lower frequency to create a **smaller 1 inductor solution**
- **ACT DME** (Differential Manchester Encoding) which **raises** the lower frequency corner
  - This helps **minimize** the inductance value and **achieve relative lower cost than existing SERDES**
- **ACT has LESS** Total Bandwidth **needed high Impedance PoC filter** = **2.77GHz**

TDD Questions:

- Have not seen TDD solution with 1 inductor operating at 10Gbps with 15meters and 4 inline connectors
  - Silicon available for 3 years with **NO** 1 inductor solution
- There has been **no impedance proposal** for TDD for **frequency of interest**
- Solutions suggested for TDD **DO NOT** offer lower frequency protection as shown in with **baseline wander issue**
  - jonsson_3dm_02_06_26_25.pdf
- **TDD has MORE** Total bandwidth **needed for high Impedance PoC filter = 2.97GHz**



	Lower Frequency Estimates	Upper Frequency Estimates
FDD SERDES	~10MHz	3GHz
ACT	~30MHz	2.8GHz
TDD	~30MHz	3GHz
802.3ch	~30MHz	2.8GHz

Summary

	ACT	TDD
Crystal-less	Proven	Theorized - Difficult
EMC	Proven robust	No data for Radar Pulse
Power	Proven Low	Great or when Equal increase in die area
Size	Lowest	Higher
Complexity	Simple and 802.3ch based	Very Difficult
25Gbps + Beyond	Lowest complexity	Higher data rate
Cable Length	Can include >15meters in spec.	Risk of collisions

THANK YOU

Questions?