Better use for reserved bits in ACT

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Introduction

- The RS-FEC used for both ACT LS and TDD have low correction capability, increasing the probability of uncorrectable error occurrence
- For ACT LS we can more reliably detect uncorrectable errors by replacing the "six vendor-specific bits" with a CRC-6 checksum to help detect uncorrectable FEC frames
- Similar CRC to detect uncorrectable FEC errors was used in 10GBASE-T, Clause 55
- The updates to the text to replace the "six vendor-specific bits" with a CRC-6 checksum will propagate through several places in the document, and the changes are detailed in the following slides

tx_RSmessage<275:0> prior to RS-FEC(50,46,6) encoder is formed as follows:

tx_RSmessage<259:0> = tx_group4x65B<259:0>.
tx_RSmessage<269:260> = OAM_field<9:0>.
tx_RSmessage<275:270> = vendor-specific_field<5:0>.

Proposed Changes

Change #1
•**Location:** Subclause 191.1.3.2, Page 63, Line 25
•**Instruction:** Change the fourth paragraph of 191.1.3.2 as follows:
•**Text:**
Next, 10 OAM bits and ~~six vendor-specific bits~~ **a 6-bit CRC field** are appended to form a 276-bit block. **The 6-bit CRC is calculated over the four 65B blocks and the 10 OAM bits as specified in 191.4.2.2.14a.** Each of these 276-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(50,46,6).

Change #2
•**Location:** Subclause 191.4.2.2, Page 97, Line 48
•**Instruction:** Change the third paragraph of 191.4.2.2 as follows:
•**Text:**
After mapping the eight XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take one group of four 65B blocks and append a 10-bit OAM field followed by a ~~6-bit vendor-specific field. When the 6-bit vendor-specific field is not used, it is recommended that it be set to 0x3F. This~~ **6-bit CRC field. This** forms the input to RS-FEC which adds 24 parity bits.

Change #3
•**Location:** Subclause 191.4.2.2, Page 98, Line 20
•**Instruction:** Change the last paragraph of Page 98 as follows:
•**Text:**
During transmission, four blocks of 65B encoded bits are appended with a 10-bit OAM field followed by a ~~6-bit vendor specific field~~ **6-bit CRC field** to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes Reed-Solomon encoders to generate and append 24 parity check bits to form 300-bit (50,46,6) RS-FEC frames.

Change #4
•**Location:** Figure 191-20, Page 98
•**Instruction:** Change the block diagram label in Figure 191-20 as follows:
•**Text:**
Training frame ~~OAM/vendor-specific~~ **OAM and CRC** bit fields)

Proposed Changes (cont.)

Change #5
•**Location:** Figure 191-21, Page 100, Line16
•**Instruction:** Change Figure 191-21 as follows:

1.In the "Aggregate 4x 65B blocks" row, change the label of the 6-bit field from ~~reserved~~ to **CRC-6**.
2.In the processing block, change the instruction from ~~Insert OAM, reserved~~ to **Insert OAM and CRC-6**.

Change #6
•**Location:** Figure 191-22, Page 101
•**Instruction:** Change Figure 191-22 as follows:

1.In the processing block, change the instruction from ~~Strip Reserved, OAM~~ to **Verify CRC-6, strip OAM/CRC-6**.
2.In the "Strip Reserved, OAM" output row, change the label of the 6-bit field from ~~OAM reserved~~ to **OAM and CRC-6**.

Change #7
•**Location:** Subclause 191.4.2.2.13, Page 102, Line 13
•**Instruction:** Change the first and second paragraphs of 191.4.2.2.13 as follows:
•**Text:**
The resulting RS-FEC frame of four 65B blocks, followed by ten OAM bits, ~~six vendor specific bits~~ **a 6-bit CRC field**, and 24 parity bits is 300 bits. See Figure 191−21 and 191.4.2.2.14 for details on PCS bit ordering and RS-FEC encoding.
The RS-FEC encoding takes the 276-bit vector, consisting of tx_group4x65B, the ten OAM bits, and ~~six vendor specific bits~~ **the six CRC bits**, and shall generate the four 6-bit parity symbols (24 bits total).

Change #8
•**Location:** Subclause 191.4.2.2.14, Page 102, Line 48
•**Instruction:** Change the final list items of the tx_RSmessage definition as follows:
•**Text:**
tx_RSmessage<275:0> prior to RS-FEC(50,46,6) encoder is formed as follows:
tx_RSmessage<259:0> = tx_group4x65B<259:0>.
tx_RSmessage<269:260> = OAM_field<9:0>.
tx_RSmessage<275:270> = ~~vendor_specific_field<5:0>.~~ **CRC_field<5:0>.**
The CRC_field<5:0> contains the 6-bit CRC computed over tx_RSmessage<269:0> as specified in 191.4.2.2.14a.

Proposed Changes (cont.)

Change #9
•**Location:** Page 102
•**Instruction:** Insert new subclause 191.4.2.2.14a (editor to renumber the result) after 191.4.2.2.14 as follows:
•**Text:**
191.4.2.2.14a CRC-6 calculation
For the low-speed path, a 6-bit cyclic redundancy check (CRC-6) shall be calculated over the 270 bits of information payload (comprising tx_group4x65B<259:0> and OAM_field<9:0>).
The CRC-6 is the remainder of the division of the payload polynomial by the generator polynomial:
g(x) = x^6 + x + 1
The coefficients of the payload polynomial are mapped from tx_RSmessage<269:0> such that tx_RSmessage<0> corresponds to the highest power term (x^{269}) and tx_RSmessage<269> corresponds to the lowest power term (x^0). The division is performed serially MSB-first. The resulting 6-bit remainder is mapped to CRC_field<5:0> where CRC_field<0> is mapped to tx_RSmessage<270> and CRC_field<5> is mapped to tx_RSmessage<275>.

Change #10
•**Location:** Subclause 191.4.2.3, Page 104, Line44
•**Instruction:** Change the third paragraph of 191.4.3.2 as follows:
•**Text:**
Following descrambling, the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into ten OAM bits, ~~six vendor-specific bits~~ **a six-bit CRC field**, and four 64B/65B blocks. **The receiver computes the CRC-6 checksum over the decoded 270 bits of information payload (comprising the four 64B/65B blocks and the ten OAM bits) and compares it with the received CRC field. If the computed CRC does not match the received CRC field, the frame is marked as invalid.** This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 191−19).

Change #11
•**Location:** Subclause 191.4.4, Page 106, Line 26
•**Instruction:** Change the second paragraph of 191.4.4 as follows:
•**Text:**
The four 65-bit blocks of the training frame, tx_group4x65B block, as defined in 191.1.3.2, are transmitted as described in 191.4.2.2.14. The four training frame 65-bit blocks are then concatenated with the 10 OAM bits, ~~six vendor-specific bits~~ **6 CRC bits**, and the 24 FEC parity bits, as shown in Figure 191−24. **The 6 CRC bits are computed over the 270 bits of the training frame (comprising the four 65-bit blocks and the 10 OAM bits) as specified in 191.4.2.2.14a.** Zeros shall be transmitted in the OAM field of the training frame.

Proposed Changes (cont.)

Change #12
•**Location:** Figure 191-24, Page 106, Line 40
•**Instruction:** Change Figure 191-24 as follows:
1.Change the column header in the training frame block from ~~v-s~~ to **CRC**.
2.Change the sub-label from ~~6-bit vendor specific~~ to **6-bit CRC**.

Change #13

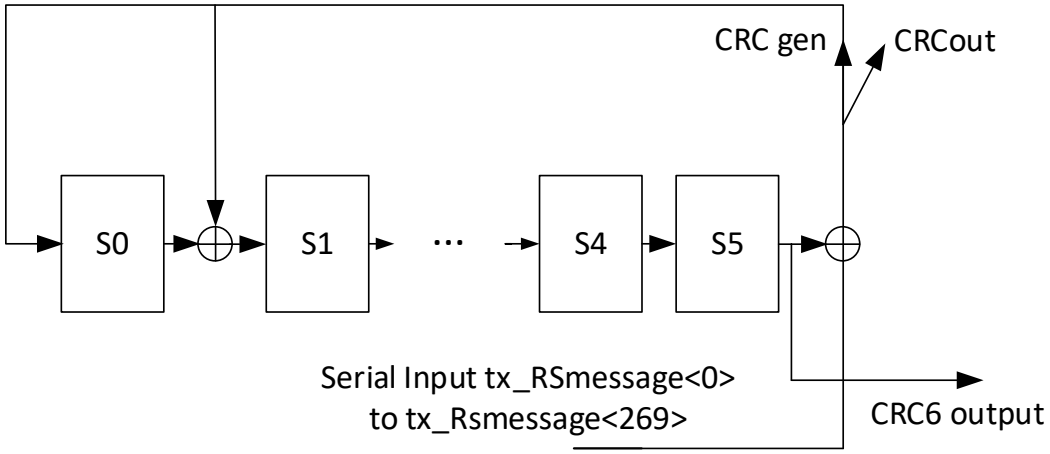
Location: Subclause 191.4.4, Page 107, Line 1

Instruction: In the training frame scrambling piecewise equation (following Equation 191–9), change the label of the third case as follows:

Text:

$$S_n = \begin{cases} Scr_n[0] \oplus \text{Infofield} & 195 \leq (n \bmod 300) \leq 259 \\ Scr_n 0 \oplus \text{OAM} & 260 \leq (n \bmod 300) \leq 269 \\ Scr_n[0] \oplus \text{~~6bit v-s~~ CRC} & 270 \leq (n \bmod 300) \leq 275 \\ Scr_n[0] \oplus \text{Parity} & 276 \leq (n \bmod 300) \leq 299 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

CRC6 Block Diagram



- The CRC6 proposed in this document is very similar to the CRC16 used in Clause 55
- The figure on the left shows the CRC6 implementation, in the same style as figure 55-27
- This figure might enhance the clarity of new Clause 191.4.2.2.14a (see change #9)
- The editor has full editorial license to decide if this figure should be included with Clause 191.4.2.2.14a

Summary

Slides 3-7 propose specific changes to the text in Clause 191

The proposed changes have minimum impact on the excising modulation

- No change to line rate
- No change to RS-FEC frame size
- No change to RS-FEC code
- No change to PMA/PMD electrical behavior
- No additional payload overhead
- No loss of interoperability


Infineon