LS_PATH I2C Traffic Analysis on 802.3dm

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Contributors

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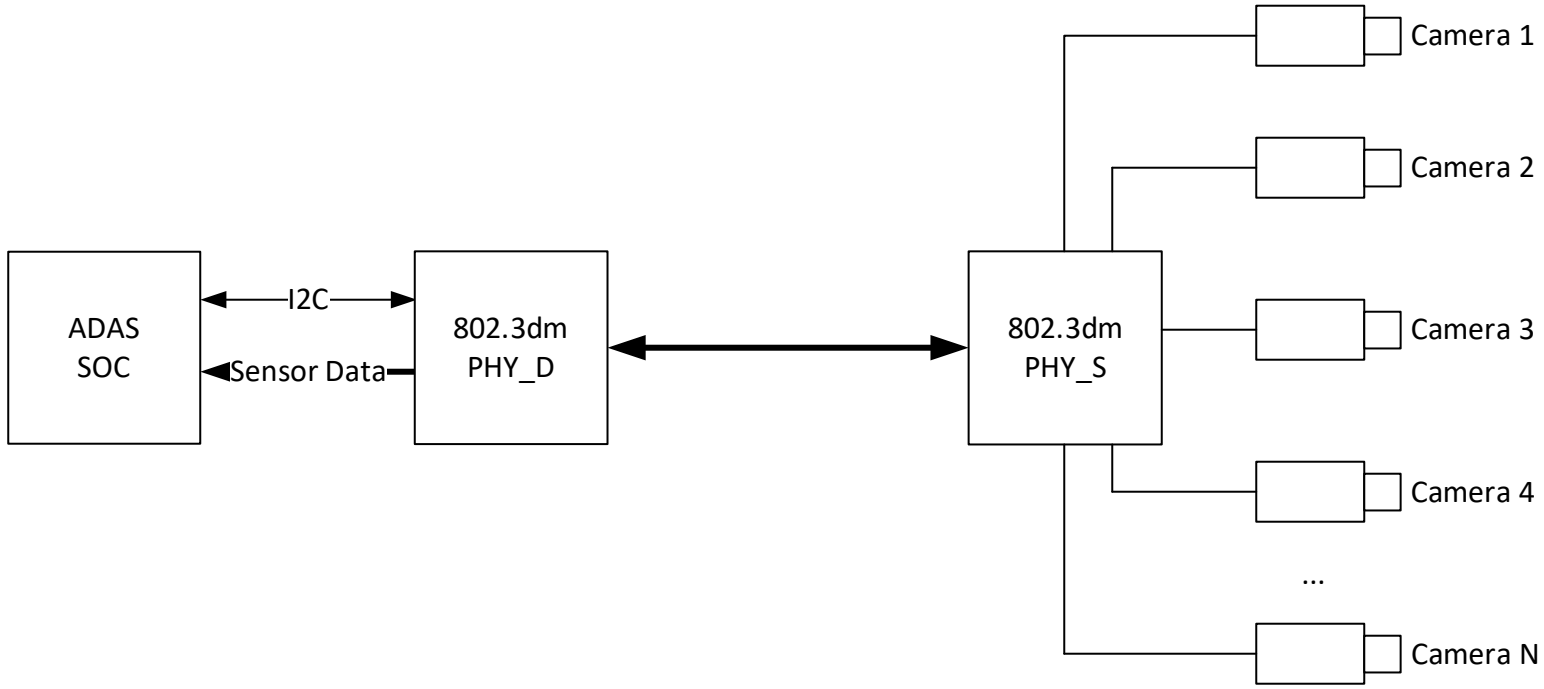
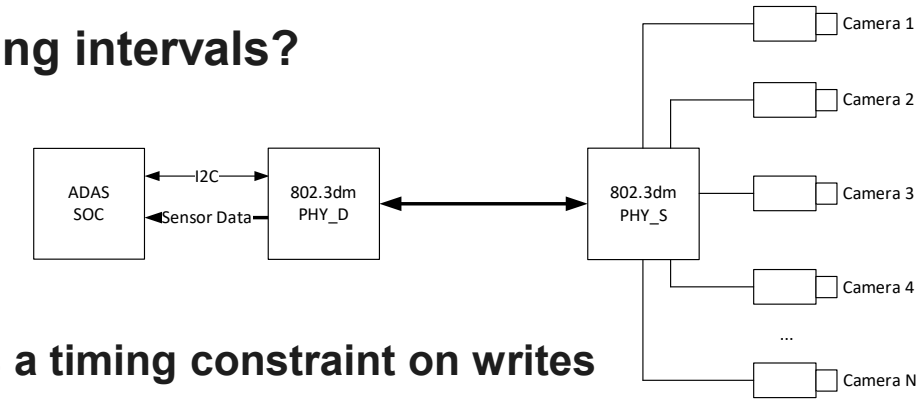
Introduction

- The LS_PATH is defined as 100Mbps for 802.3dm.
  - Is 100Mbps bandwidth on the LS_PATH enough, or is it a limiting factor for an aggregator?
- I2C traffic to and from imager ICs and imager peripherals is a critical consideration when evaluating the bandwidth utilization and bandwidth requirements of an 802.3dm deployment.
- Is I2C limiting the number of sensors that can be connected to an aggregator?

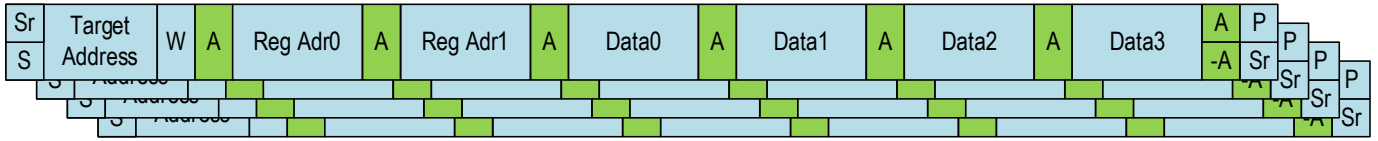


Assumptions and Analysis

- 802.3dm HS_PATH camera->SOC, 100Mbps LS_PATH SOC->camera
- **How many cameras can be aggregated with synchronized blanking intervals?**
  - **1Mbps I2C connected to PHY_D**
  - **One imager 60fps/15% blanking + other imagers 30fps/15% blanking**
  - **All frame writes (Exposure/Gain) must occur during blanking interval**
  - **Other writes and reads can occur at any other time**
  - **This represents a 'Worst Case' condition as the blanking interval puts a timing constraint on writes**

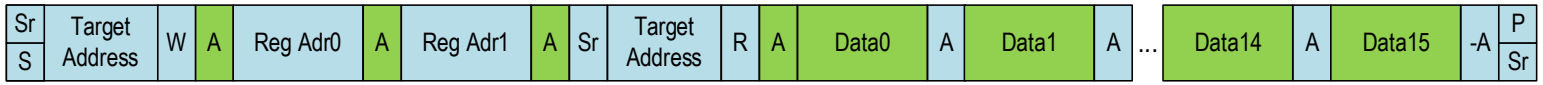


– From SOC controller to each imager target:
  – Firmware download of 5KB from SOC to each imager for initialization
  – 3 x 32 octet I2C write commands (3 x 4 octets each), per frame, per imager, 60 fps (2.5ms) / 30fps (5ms)
  – Analog Gain/Digital Gain
  – Integration time / Coarse Exposure
  – Mode Select / Streaming Control



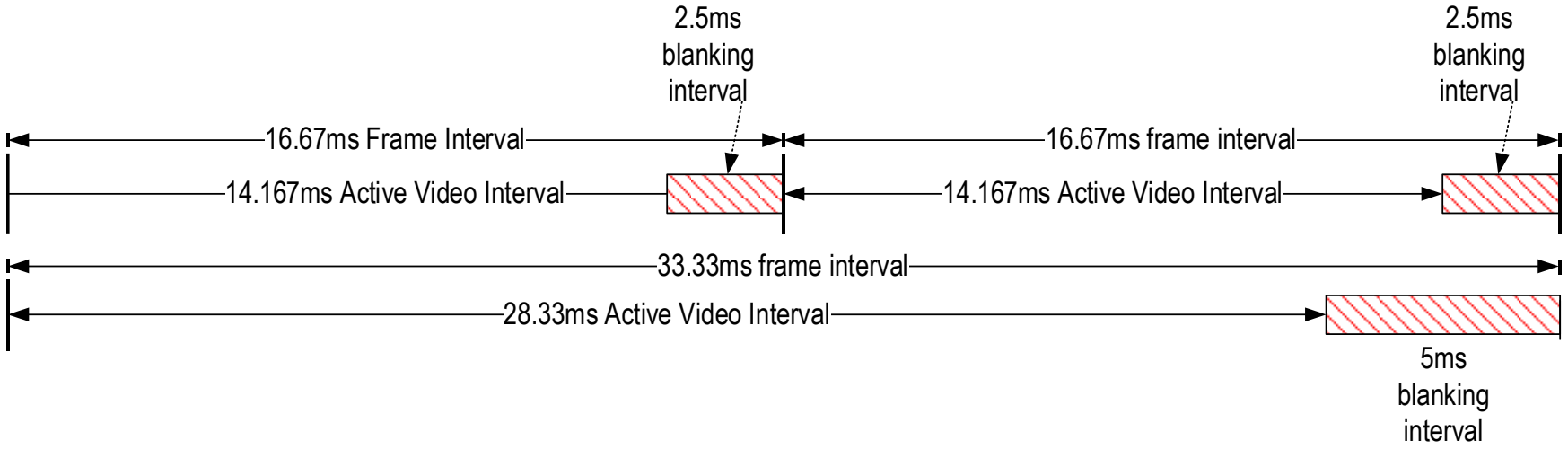
  – Status read of 16 octets as a single burst read for safety information every FTTI of 16.67ms
    – GSR (1 register)
    – ESM (2-3 registers)
    – Frame Count/Heartbeat (1 register)

A single block read



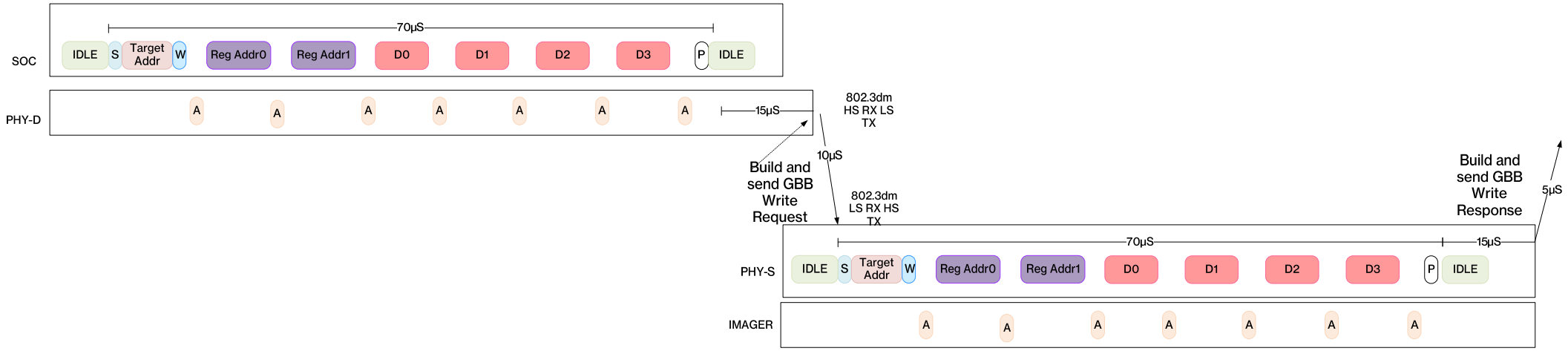
Imager Writes Using 1722-2025 Annex M, Worst-Case Condition

- 1 x 60fps, 15% blanking, N-1 x 30 fps, 15% blanking
- All imager control writes per frame for all imagers occur during the blanking intervals
  - Image registers control exposure, gain, etc. Changes outside of blanking may cause artifacts



- Use IEEE-1722 Annex M (GBB) write request/write response packets per imager per blanking
  - 1 GBB write request each for
    - Analog Gain/Digital Gain
    - Integration time / Coarse Exposure
    - Mode Select / Streaming Control
  - 1 GBB write response per write request

Imager Writes using GBB

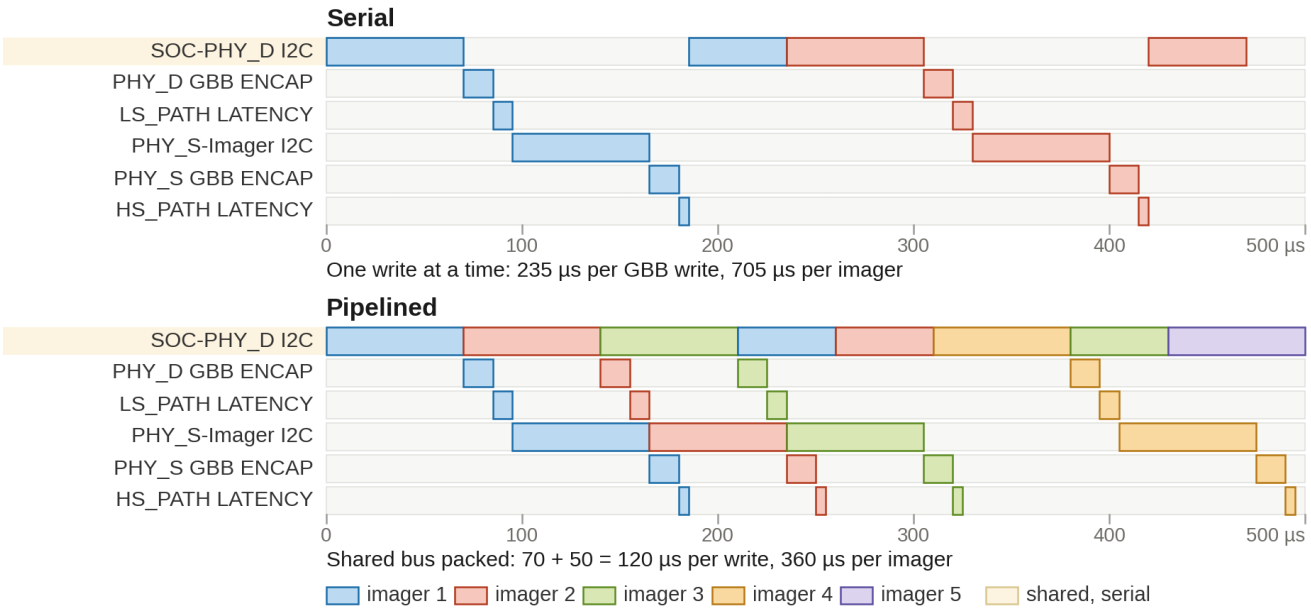


– The time for each imager write is composed of:

Stage	Time	Resource
SOC->PHYD I²C write	70µs	SOC<->PHY_D I²C shared, serial
Build/Send GBB write request	15µs	PHY_D packetization
LS_TX transmission	**10µs**	**LS_PATH**
PHY_S-> Imager I²C write	70µs	Per-camera I²C, parallel
Build/send GBB Write Response	15µs	PHY_S packetization
PHY_S->PHY_D latency	5µs	HS_PATH
SOC status read from PHY_D	50µs	SOC<->PHY_D I²C shared, serial
Total	235µs	

Number of Imagers Supported Writing During Blanking

- The SOC<->PHY_D I²C bus occupancy is only 120µs
- Once a write is kicked off, the writes may be pipelined
- With pipelining, the number of imagers supported increases



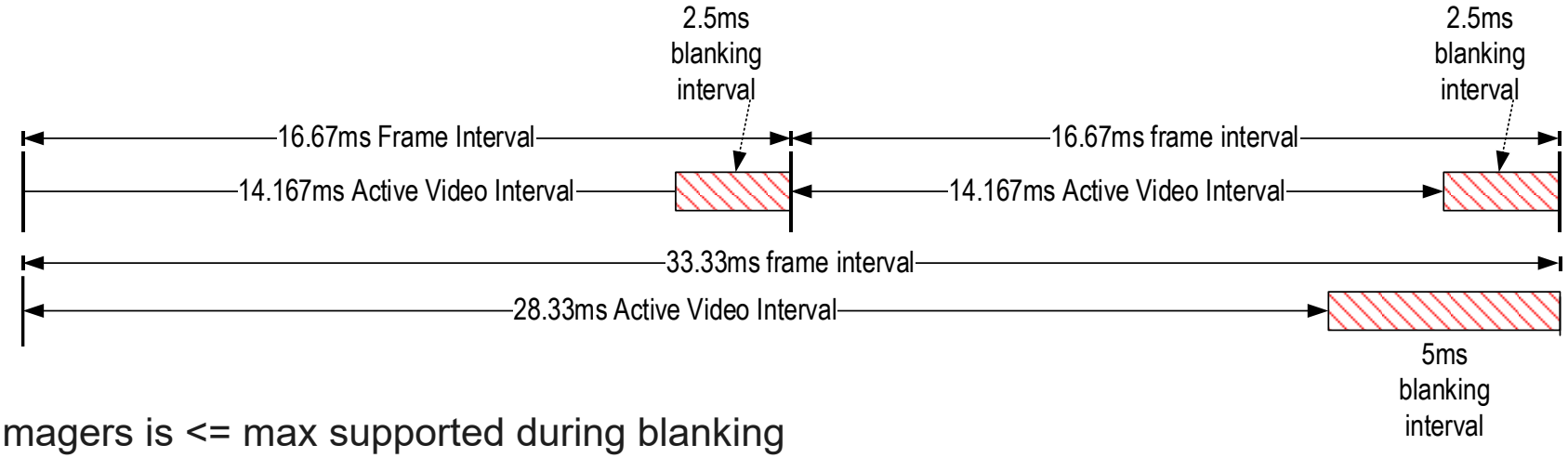
Case	Elapsed Time I2C Writes per Imager	Imagers supported
Serialized, 3 GBB writes per imager	3 GBB writes x 235us/GBB write = 705µs	**7.** If 1 imager is 60fps, **6**
Pipelined, 3 GBB writes per imager	3 GBB writes x 120us I2C bus occupancy = 360µs	**13.** If 1 imager is 60fps, **12**

Imager Safety Reads

- Status read of 16 octets as a single burst read for safety information every FTTI of 16.67ms
  - GSR (1 register)
  - ESM (2-3 registers)
  - Frame Count/Heartbeat (1 register)
    - These registers are contiguous

  A single block read

  - Register read during normal frame interval (14.167ms)



  - Assume that # of imagers is <= max supported during blanking

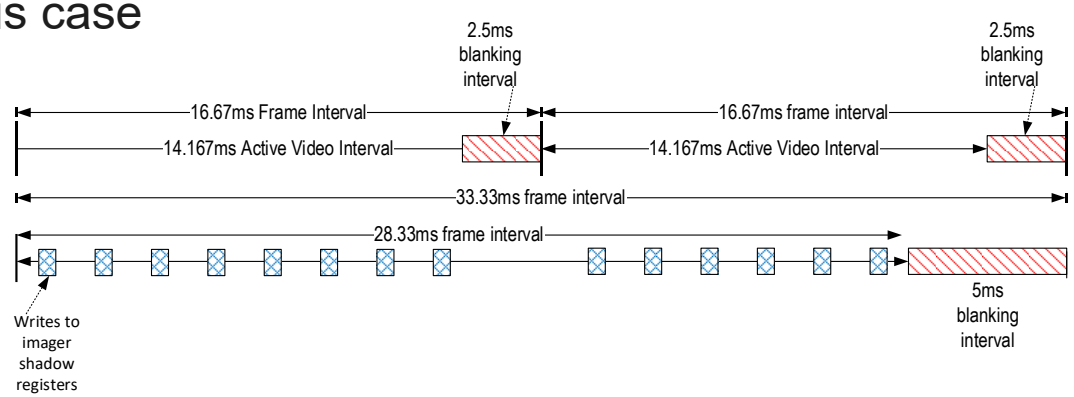
- 12 imagers with 1 GBB FTTI I2C read packet each * (8bits/Byte*(64B Frame +8B Pre/SFD + 12B IPG)) x 2 (read request / read response) = **16.128kbits**
- Capacity of LS_PATH during Active Video Interval = (14.167ms)*100e6 = **1.4167Mbits**
- I2C read traffic on LS_PATH for safety during is **< 1.2% of LS_PATH BW** during the Active Video Interval
- **100Mbps LS_PATH fully supports imager safety reads**

What Else?

- The imager writes during blanking and safety reads only occupy a small fraction of LS_PATH bandwidth
- LS_PATH bandwidth can be used for:
  - Additional I2C control / reads to the imagers which are not exposure based or safety-related
  - SPI traffic to radar MMICs
  - EEPROM reads and writes for radar and imaging
  - Lens heater/MMIC de-icer control/monitoring/watchdog
  - LED Driver Control (Interior Camera)
  - PMU control/monitoring
  - Overvoltage/Undervoltage (OV/UV) monitoring

Shadow Registers

- The previous analysis was a worst-case analysis where the I2C register writes for the next frame had to occur during the blanking interval
- The requirement for imager writes for gain and exposure during blanking is a real requirement, however, most modern imagers have **shadow registers**
  - PHY_D performs I2C writes to imager shadow register during Active Frame Interval
  - Shadow registers on the imager post from shadow to active after the Frame Sync signal
- For example, 14 x 720 µs intervals in the Active Frame Interval using pipelined GBB writes
  - **28** imagers supported in this case



- There is enough headroom to support any 2.5/5/10Gbps HS_PATH aggregation with 100Mbps LS_PATH bandwidth

Conclusion

- 100Mbps LS_PATH with GBB I2C does not limit the number of imagers which may be connected to 802.3dm PHY_S aggregators
- 100Mbps LS_PATH fully supports image aggregator applications