Further Thoughts Regarding Timeline Considerations



A Leading Provider of Smart, Connected and Secure Embedded Solutions

Supporters

- Scott Muma (Microchip)
- Claude Gauthier (NXP)
- Kamal Dalmia (Aviva Links)
- Yasuhiro Kotani (DENSO)
- Yoshifumi Kaku (DENSO)



Timeline Considerations Overview

As noted in gorshe_3dm_01a_2410:

- ☐ The number of cameras in new cars is undergoing a significant increase
 - It is expected that around 12 cameras per car will soon become typical
- ☐ There is a finite time window for P802.3dm to have maximum market success
 - Camera systems are currently being designed into new cars and car models.
 - The longer it takes to complete P802.3dm, the greater the likelihood that an alternative will become the de facto standard due to extensive deployment
 - If the alternative adequately satisfies the application requirements, there may be little incentive to change over to P802.3dm



Timeline Considerations - Examples

- ☐ Specific examples of the timeline challenges with ACT
 - The ACT US proposal used Differential Manchester Encoding (DME) with loop timing and an LPF at the camera instead of an echo canceler or equalizer:
 - The proposed 100 Mbps US line rate requires the camera side to lock loop timing with a low-frequency reference signal to generate an accurate highfrequence (5 Gbps)
 - Locking a 5 Gbps line rate to a 100 Mbps like rate would require 50 times the accuracy
 - The typical oscillator's random jitter makes it difficult to ensure the accuracy of the 5 Gbps signal
 - The challenge with using an LPF to suppress the echo on both sides is adjusting the passband cutoff frequencies
 - A wider passband causes less distortion to the DME signal, but more echoes
 - A narrower passband can suppress echoes, but distorts the DME signal, impacting loop timing
 - A quantitative performance analysis is required, with full system-level simulations.



Timeline Considerations

- ☐ As noted in multiple contributions to the October and November ISAAC meetings:
 - TDD-based solutions have proven advantages and a successful deployment history
 - The issues and challenges being addressed by IEEE P802.3dm have been extensively researched in ASA to arrive at interoperable solutions that have been demonstrated to satisfy the ISAAC objectives
 - ASA participants represent multiple entities, including end users, chip and equipment manufacturers and cable vendors
 - Multiple contributions to this meeting include proposals that leverage the ASA studies and conclusions
 - Hence, leveraging the ASA PHY work allows IEEE P802.3dm to avoid the delays associated with "re-inventing" and verifying the wheel of a new approach



Timeline Considerations

- ☐ Timeline considerations should include implications beyond the IEEE 802.3dm publication date
 - Leveraging the ASA PHY work also makes it straightforward for the resulting P802.3dm standard to inherit the existing ASA eco-system
 - Adopting a TDD solution that leverages ASA allows accelerated device development
 - The maturity and feasibility of the ASA approach has been demonstrated with interoperable prototype devices
 - This, combined with the lower complexity of TDD (e.g., simpler analog front end and no need for echo cancelling) enables device designs to begin much earlier in the P802.3dm cycle



Recommendation and Proposal

- New technical approaches will inherently slow the progress of P802.3dm due to the need for extensive simulation, testing and verification by multiple unaffiliated individuals
- ☐ ASA specifications are already available as adequately mature standards that could be leveraged towards the P802.3dm baseline
 - Adopting an ASA-leveraged TDD approach would also enable accelerated implementation and availability of interoperable devices
- ☐ In order to maximize the likelihood of P802.3dm market success, we propose that the Task Force focus on leveraging ASA-based technology and growing ecosystem (e.g., >160 member entities) as much as possible



Thank You

