A Simplified Training Flow for 5/2.5G

Alireza Razavi

Motivation

- Objective :
  - Demonstrate that the 5/2.5G training sequence can be significantly simplified
  - Lowering the implementation cost, reducing the failure rate, and improving cross-vender interoperability

- This is a follow-up presentation to
  - https://www.ieee802.org/3/dm/public/0925/Razavi_3dm_01a_092025.pdf
  - It is a work in progress

Training signaling in 5/2.5G

- During 5/2.5G training, PMA uses the same signaling through the training
  - PAM2 signaling in High Data Rate (HDR) direction
  - DME signaling in Low Data Rate (LDR) direction
- The PCS determines the interpretation of the signals
  - Training signals include SEND_T, and SEND_N
- COUNTDOWN/TX_SWITCH are used when switching from SEND_T to SEND_N

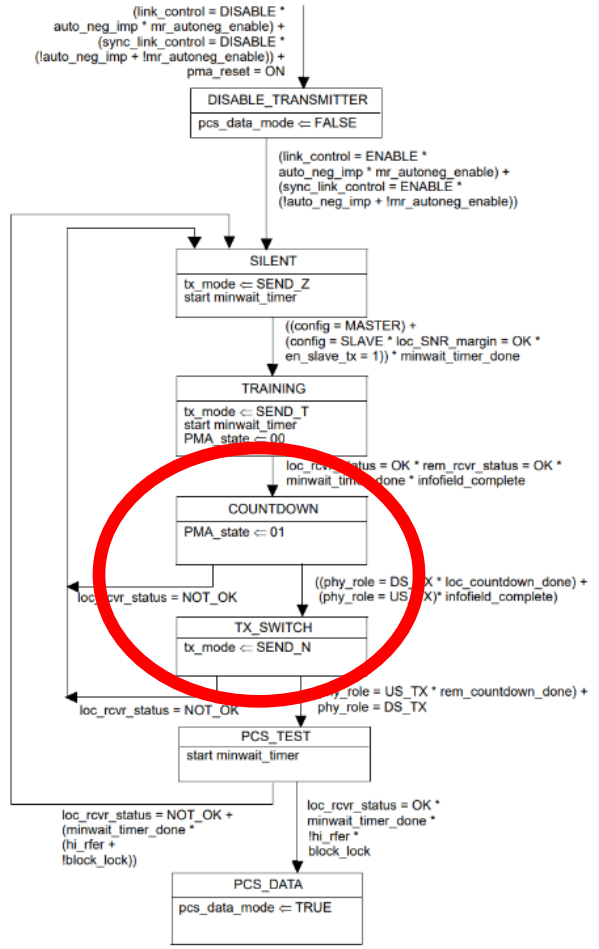


Figure 201–15—PHY Control state diagram

PMA Training: The same signaling during training

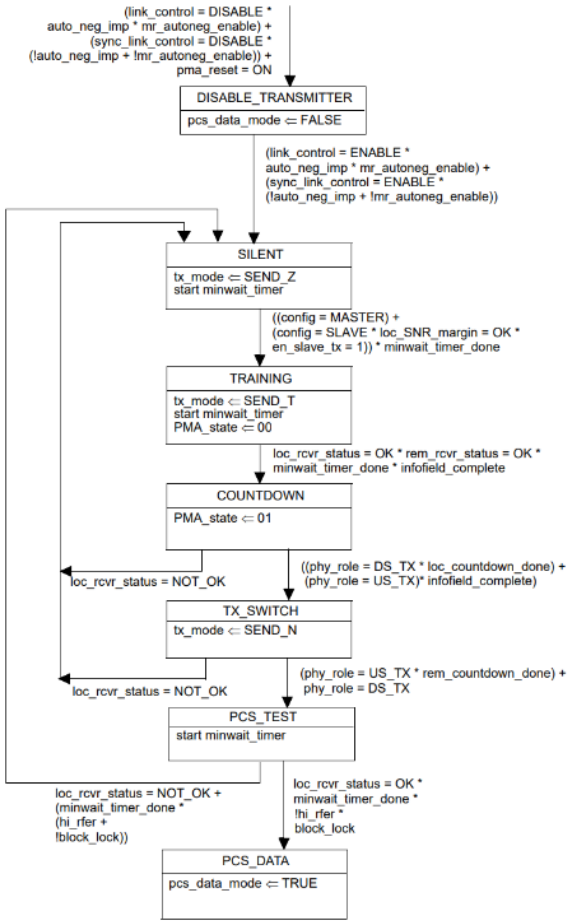
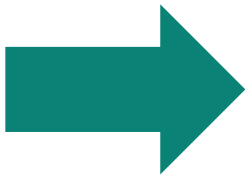
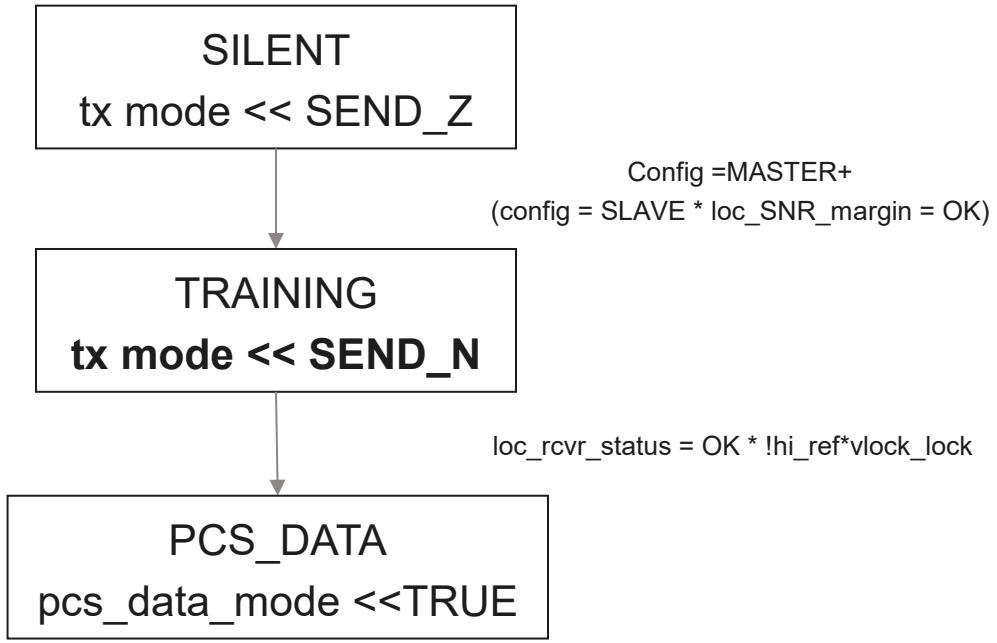


Figure 201–15—PHY Control state diagram





PCS signaling during the training

- These sets of data are exchanged during training
  - Messages about the training state machine
  - Frame boundaries and counters: PFC24/DataSwPFC24
  - Preferred PHY settings : interleaver, pre-coder,…

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 149–27—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149–28—Infofield COUNTDOWN format

Messages are NOT required when training starts with SEND_N

- loc_rcvr_status :
  - only used to transition into COUNTDOWN state
  - No COUNTDOWN means no need for this message
- en_slave_tx :
  - There is no echo canceler in ACT
- timing_lock_OK
  - This is just an informative bit. Slave does not transmit till its timing recovery is locked

Table 149–10—Infofield message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 149–11—Infofield message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

No COUNTDOM when training starts with SEND_N

– No need for info-field COUNTDOWN format

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 149–27—Infofield TRAINING format

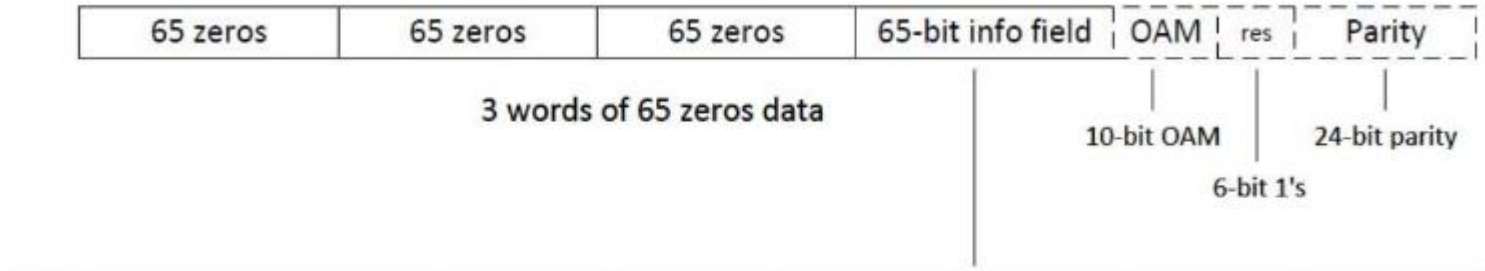
PMA_state = 01

octet 1	octet 2	octet 3	octe…5/6	…et 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 149–28—Infofield COUNTDOWN format

Detecting the frame boundaries when training starts with SEND_N

- OAM is placed in pre-determined position
- This can be used to detect the start of the frame



C/D								
1	Block	D0	D1	D2	D3	D4	D5	D6
1	0x5A	Reserved	Reserved	Reserved	Message	PHY Capability Bits		

Figure 201–14—Training frame

Exchange of PHY capabilities when training starts with SEND_N

- There is no option for PHY settings in the LDR direction
- There are PHY settings that will be set by PHY capability bits in the HDR direction
  - It is not clear how many of PHY settings are going to stay in the HDR direction
  - Capability bits can be transmitted by OAM
- The HDR receiver can detect if these settings have been applied

Table 149–12—PHY Capability Bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	InterleaverDepth		PrecodeSel		SlowWakeRequest	EEEen	OAMen

PMA/PCS Training: The training can be simplified significantly

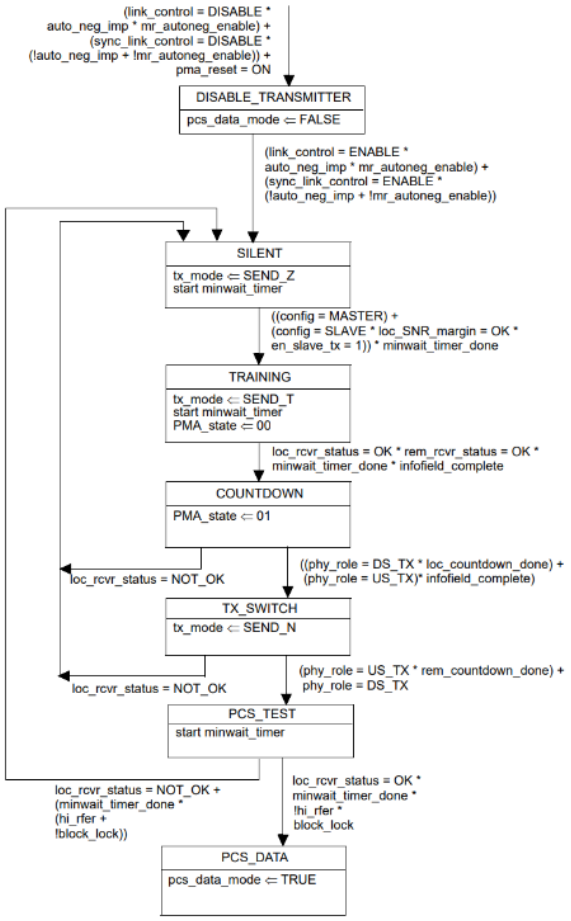
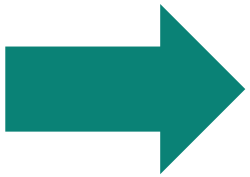
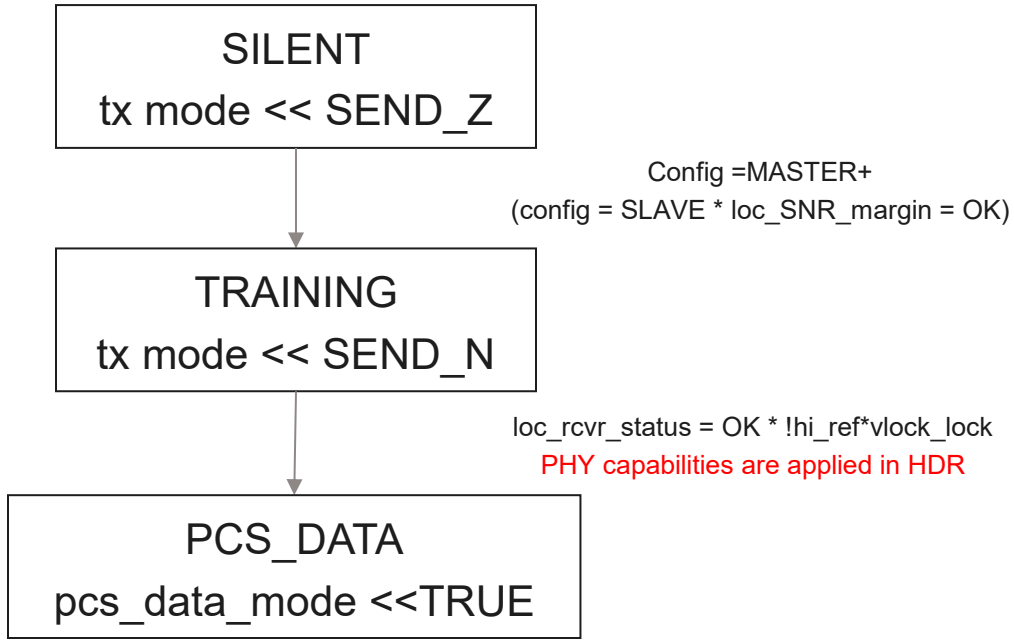


Figure 201–15—PHY Control state diagram





Conclusion

The 5/2.5G training sequence can be significantly simplified

Looking forward for your comments and feedback