Complexity Considerations for Camera Systems

IEEE P802.3dm
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Agenda

1. Motivation
2. Relevant Sub-systems
3. Complexity drivers
4. Complexity Analysis of example systems
5. Comparison
6. Conclusions

Motivation

- .3dm PAR contains in “Need for Project: (...) end-nodes are highly constrained on complexity and power (...)” [1]
- There have been multiple presentations in ISAAC TF/ .3dm on camera ECU complexity, covering various aspects of camera system design
  - camera size and imager integration [2], package and PCB size [3], crystal-less operation [4], PoC/ PoDL filter design [5]
- There is uncertainty in which directions, optimization is required on order to meet “complexity reduction” goals stated in .3dm PAR
- Multiple directions have been considered, such as: silicon area for Camera-side PHY, reduction of PoC/PoDL coupling circuitry, camera-side PHY peripherals (e.g. crystal-less)

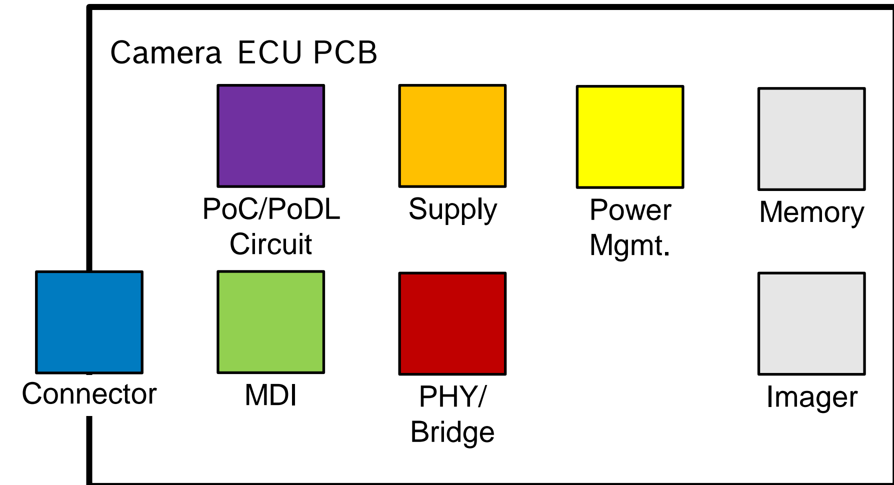
- **This contribution intends to give orientation in terms of which aspects are worth being optimized to have a relevant impact from system integration perspective**

[1]: P802.3dm PAR ec-24-0014-01-00EC-draft-ieee-p802-3dm-par.pdf
[2]: “Call For Interest (CFI) consensus meeting presentation” CFI_01_0723.pdf
[3]: “Automotive cameras and size” broedel_matheus_dm_01_size_07152024.pdf
[4]: “Link Synchronization for Crystal-less Camera Links” Zherebtsov_razavi_Ragnar_3dm_01_Jan_2025.pdf
[5]: “From Concept to Circuit: Designing Effective PoC Filters” Houck_3dm_02_0121_5.pdf

Relevant Electronics Sub-systems

Sub-systems

- Power Supply
  - DC/DC converter
  - Provisioning of n supply rails
  - Power monitoring
  - (Load-dump HSS)
- Power-over circuitry
  - Inductors, coupling, ...
- Connector
- PHY/ Bridge
  - PHY-Chip
  - PHY-Peripherals
    - Clock, Decoupling
- (Imager) – not considered
- (Imager Memory) – not considered



Good Question for Study Group – Can we enable a more efficient Ethernet solution?

A communication standard motivates combination of image sensor and transceiver in one package.

Main camera Bill of Material (BOM) items:

- PCB
- Power supply
- PoC circuitry
- Imager
- Communication chip
- Housing
- Wiring
- Connector
- Lens (barrel)

PCB / Ima ger / PWR / COM → PCB / Ima ger / PWR

An efficient communications chip (COM) is essential for competitiveness with the incumbent technologies. A power and complexity-efficient Ethernet standard can enable:

- Fewer chip packages on the PCB
- Smaller footprints with fewer communications interfaces, lower power, and reduced cost
- Reduced PCB sizes with fewer layers

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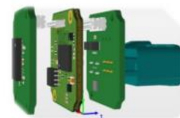
[1]: "ISAAC, Call For Interest (CFI) consensus meeting presentation", 11 July 2023 https://www.ieee802.org/3/cfi/0723_1/CFI_01_0723.pdf

In first approximation, complexity can be measured by:

- Number of passives
- Sub-system PCB footprint

Analysis of example systems

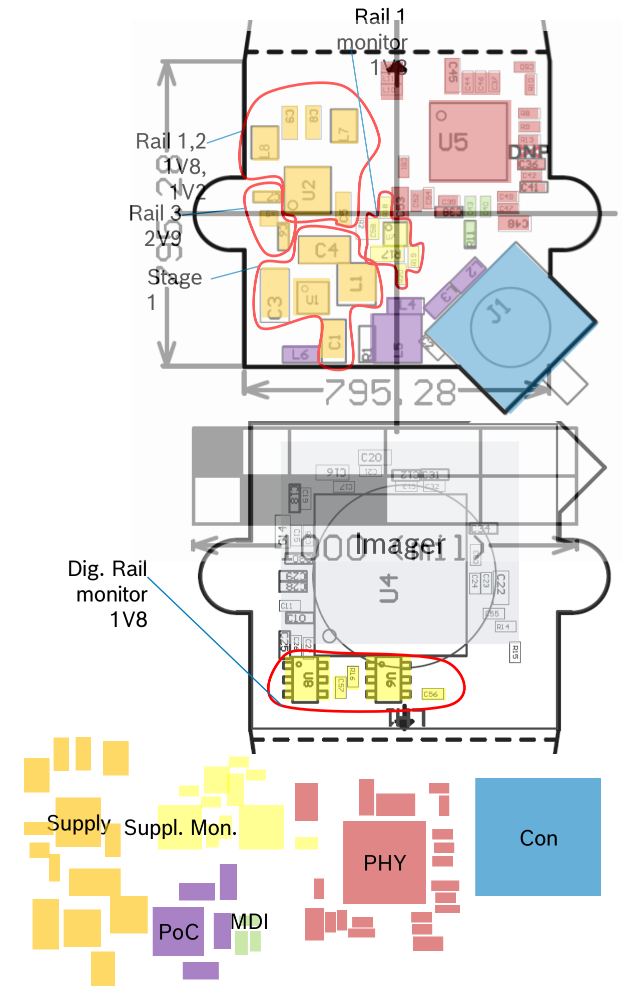
- Incumbent Reference design
  - single-PCB design, no PMIC used, in general comparable to a state-of-the-art camera design
- Ethernet (IEEE 802.3ch w/ STP)
  - 3-PCB prototype (connector, PHY, Imager),
  - slightly larger overall footprint,
  - debugging-aspects not covered in comparison
  - more details, already shown in [1]
- Ethernet (IEEE 802.3ch w/ Coax) 
  - early 3-PCB prototype,
  - slightly larger overall footprint,
  - debugging-aspects not covered in comparison

[1]: "Measurements and Simulations on MDI Return Loss including PoC/PoDL", 11 July 2023 https://grouper.ieee.org/groups/802/3/dm/public/adhoc/101024/strohmeier_dm_measure_sim_rl_101024_v03.pdf

Complexity Analysis - Incumbent Solution [1]

	Comment	# Parts	PCB Area
Power Supply	2 rails imager 1 rail serializer **3 rails total**	14	$\approx 101\ \text{mm}^2$
Power Management	-	11	$\approx 43\ \text{mm}^2$
PHY	4 Gbps	1	$\approx 26\ \text{mm}^2$
PHY-peripherals	no crystal, passives only	24	$\approx 109\ \text{mm}^2$
Power-over-x	L5 rather large, 2 ferrites should be sufficient	5	$\approx 26\ \text{mm}^2$
Imager	-	30	$\approx 219\ \text{mm}^2$

Power Supply (no. of supply rails)
and
PHY peripherals are most relevant Sub-Systems



[1]: "SerDes Reference Design" https://www.ti.com/tool/TIDA-020002

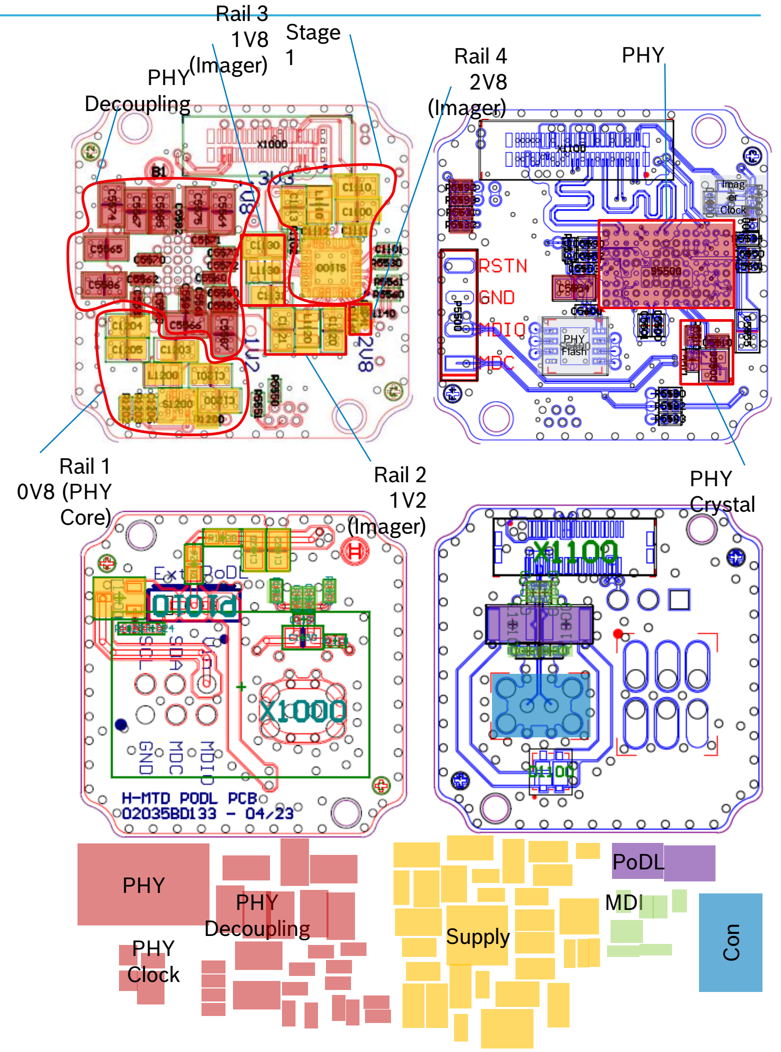
Complexity Analysis - 802.3ch (STP)

	Comment	# Parts	PCB Area
Power Supply	3 rails imager (2V8, 1V2, 1V8) 3 rails PHY (1V8, **0V8**, 1V2) **4 rails total**	29	$\approx 238\ \text{mm}^2$
Power Management	included in power management IC	-	-
PHY	5GBASE-T1	1 Active 27 Passive	$\approx 234\ \text{mm}^2$
PHY-peripherals	crystal (+4 components)	1 Active 4 Passive	$\approx 20\ \text{mm}^2$
Power-over-x	minimalistic	2 Inductors 7 HSS	$\approx 27\ \text{mm}^2$
Imager	-	-	-

Additional supply rail adds complexity

Overall PHY footprint is rather large

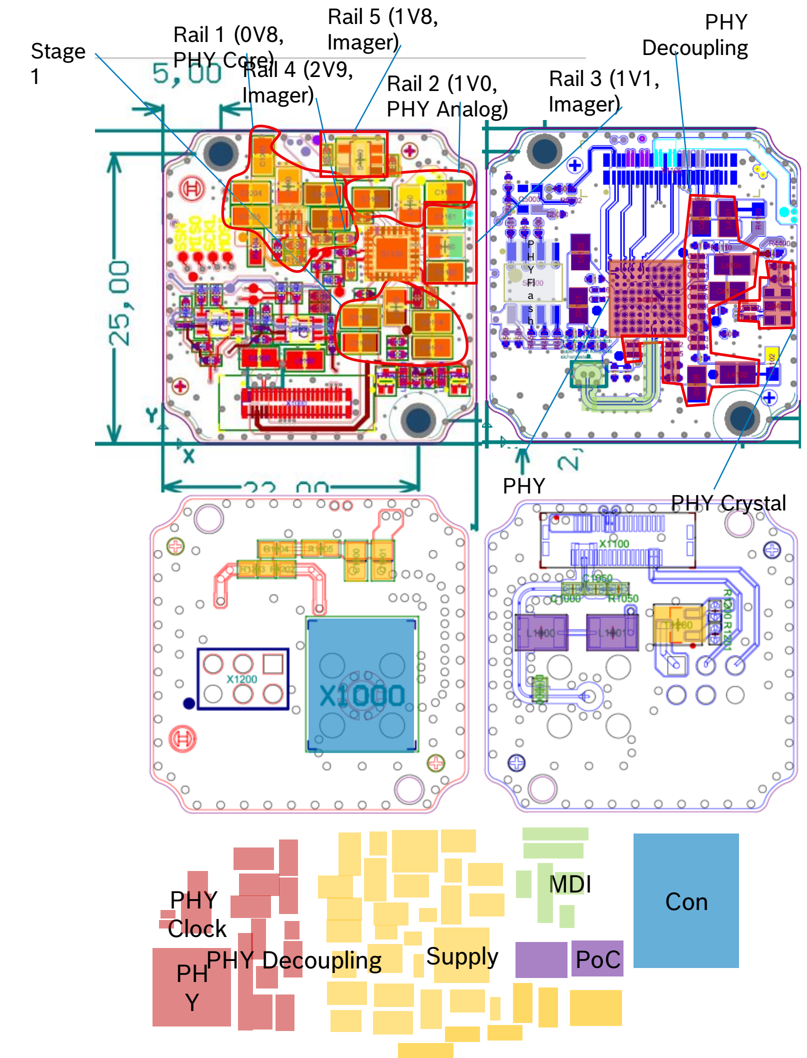
Need for crystal has



Complexity Analysis - 802.3ch (Coax)

	Comment	# Parts	PCB Area
Power Supply	3 rails imager (2V9, 1V1, 1V8) 3 rails PHY (**<u>0V8, 1V0</u>**, 1V8) **5 rails total**	2 active 26 passive	$\approx 301\ \text{mm}^2$
Power Management	included in power management IC	-	-
PHY	5GBASE-T1	1 active 20 passive	$\approx 142\ \text{mm}^2$
PHY-peripherals	crystal (comp.)	1 active 4 passive	$\approx 18\ \text{mm}^2$
Power-over-x	minimalistic	2 Inductors 7 HSS	$\approx 32\ \text{mm}^2$
Imager	-	-	-

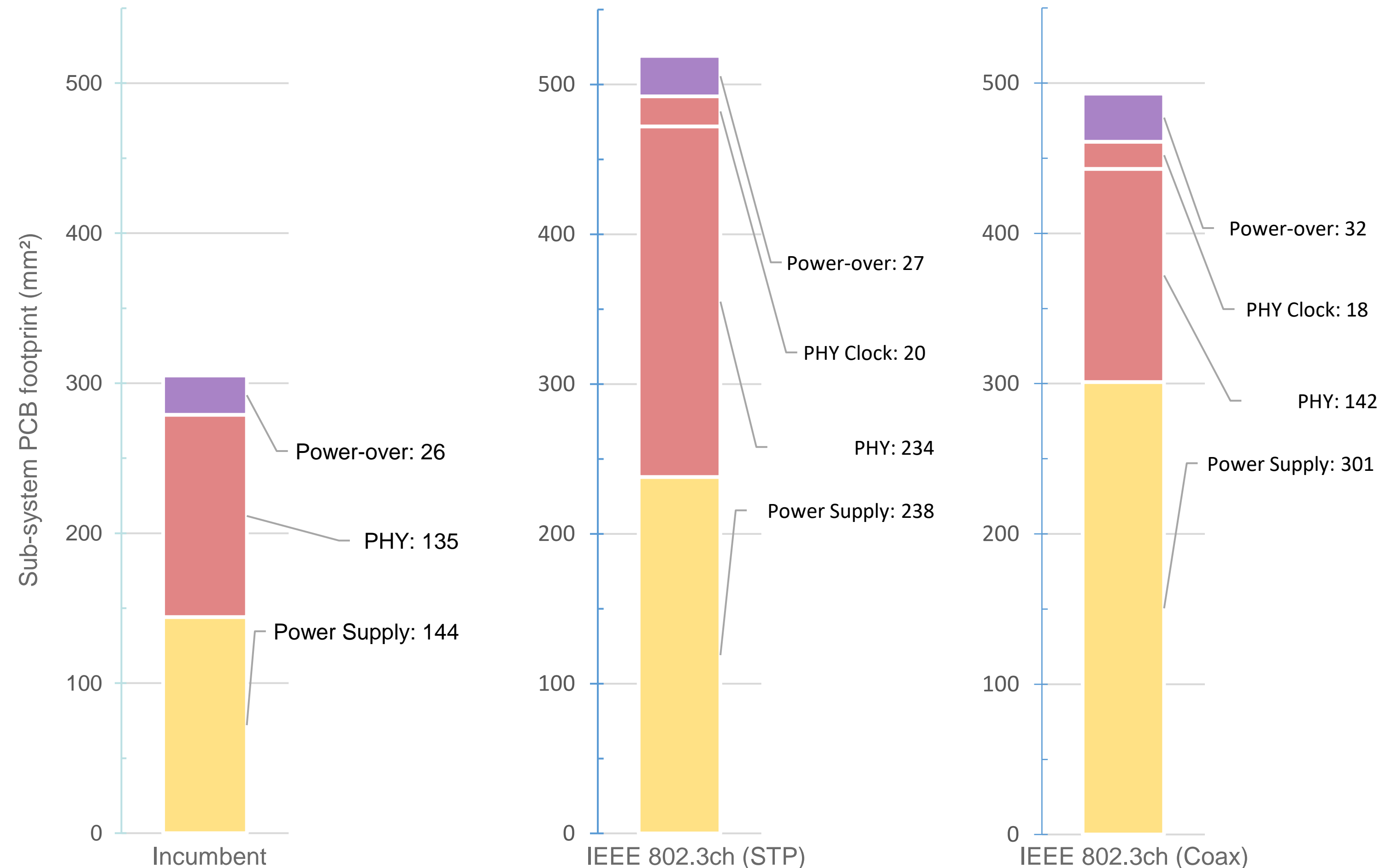
Additional supply rail adds complexity
Overall PHY footprint is rather large



Comparison - Main complexity drivers

- Incumbent solutions allow for low footprint PHY integration (approx. factor 2)

- Main complexity drivers for system implementations of .3ch are
  1. Number of supply rails
  2. PHY-Size
  3. PHY-Peripherals (discretes)
  4. PoC/PoDL circuitry
  5. PHY-Clock circuitry



Conclusions

For what should .3dm be optimized to have an impact on camera ECU complexity?

IEEE 802.3dm should (in descending order):

1. Allow for implemenatation with **low number of supply rails (matched with typical imager rails)**
2. Allow for implementation with **low pin count (small PHY/Bridge footprint size)**
3. Allow for **minimal footprint Power-over filters**
4. Allow for **crystal-less operation**
5. Allow for **minimalistic MDI** (no discrete filters, no CMC)

Thank You!