



Complexity of ACT/GMSLE Implementations

Contribution to 802.3dm Task Force

June 26, 2025

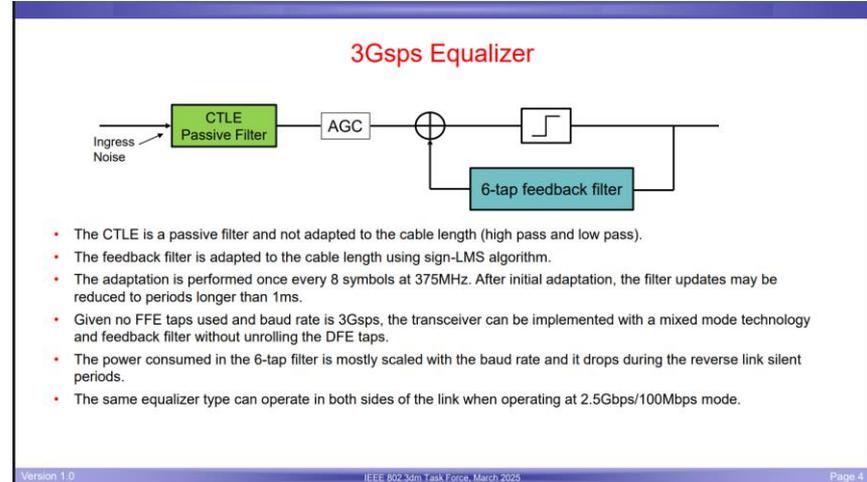
Ragnar Jonsson - Marvell

Introduction

- This presentation shows a high-level evaluation of ACT/GMSLE PHY complexity
- What is presented here are simulation results that demonstrate that
 - a relatively low complexity receiver can be used for the high data rate direction
 - a very low complexity receiver can be used for low data rate direction
- Key observation is that echo is not a predominant factor in limiting the performance or increasing the complexity of the ACT/GMSLE PHYs
 - Measurements taken from ACT-based PHY silicon confirm that no echo cancelation is needed for either the low-speed receiver in the camera or for the high-speed receiver on the network side

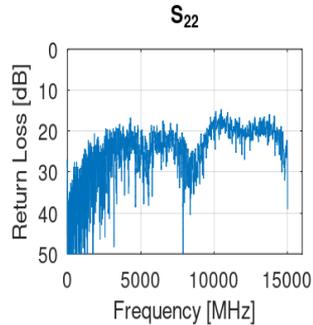
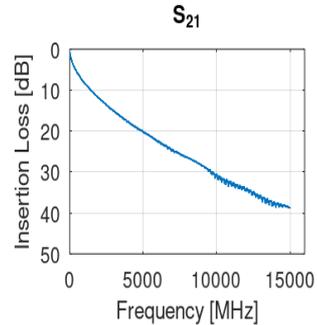
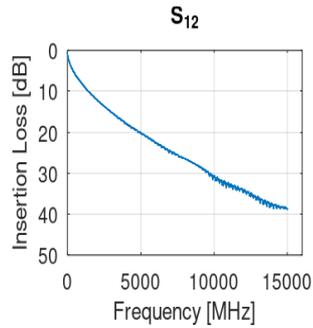
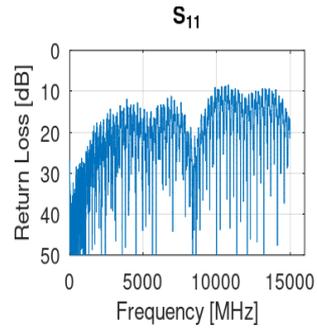
Simple High Data Rate Receiver

- It was suggested in [Chini_3dm_02b_0325.pdf](#) that relatively simple PMA receiver could be implemented for 3Gbps line rate (see figure on the right)
- Because echo is not a predominant problem in ACT/GMSLE, same equalization scheme can be used for the 2.5Gbps high data rate receive
- The only difference is that the ACT/GMSLE PHY would be operating at 2.8Gbps line rate, compared to 3Gbps line rate for TDD

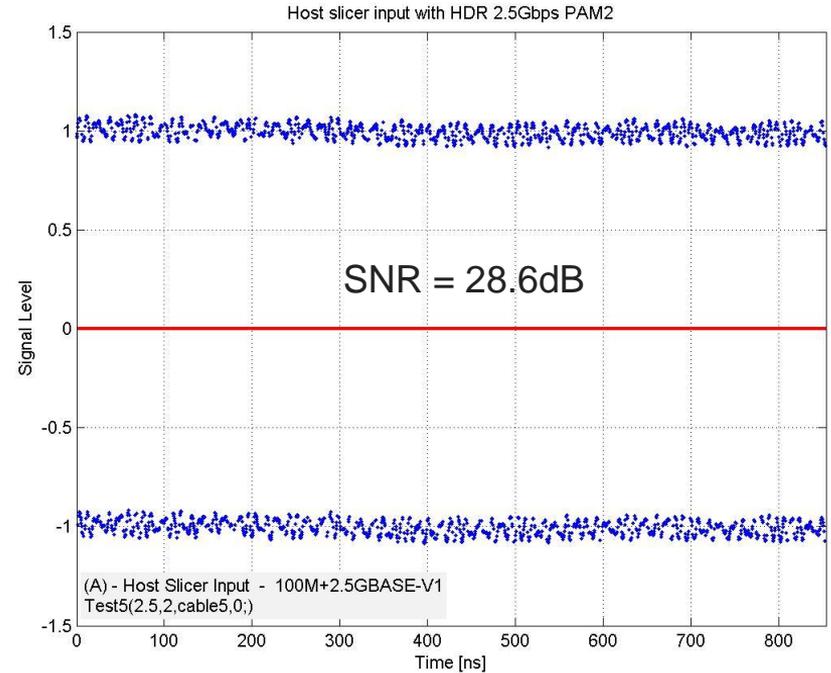


From https://www.ieee802.org/3/dm/public/0325/Chini_3dm_02b_0325.pdf

15m Coax with 4 Typical Inline Connectors

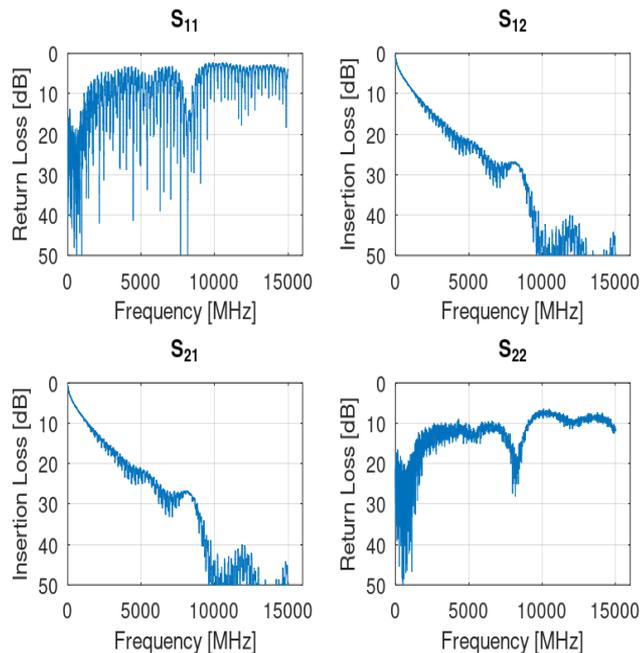


HP-cutoff = 0.1MHz

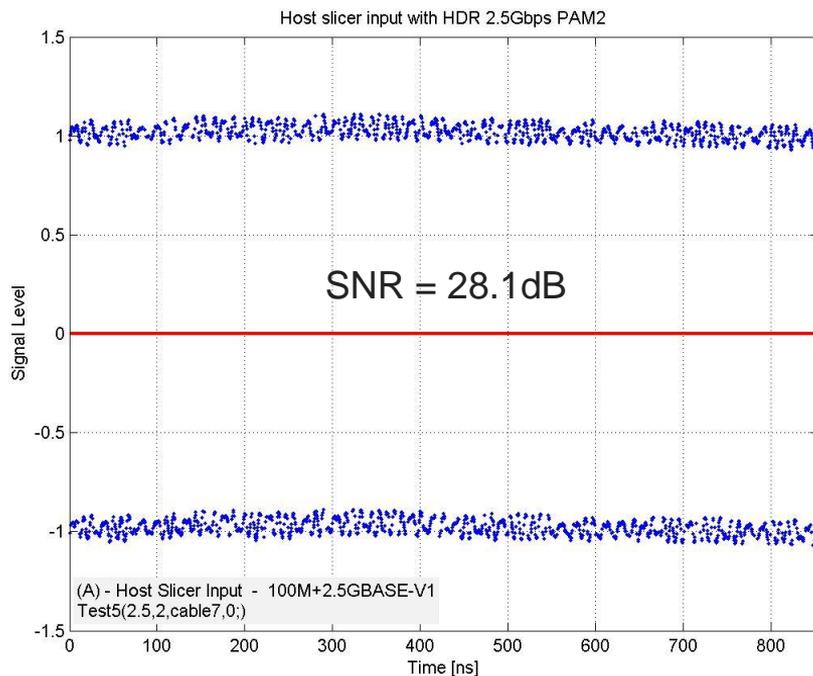


15m Coax with 4 “Ugly” Inline Connectors

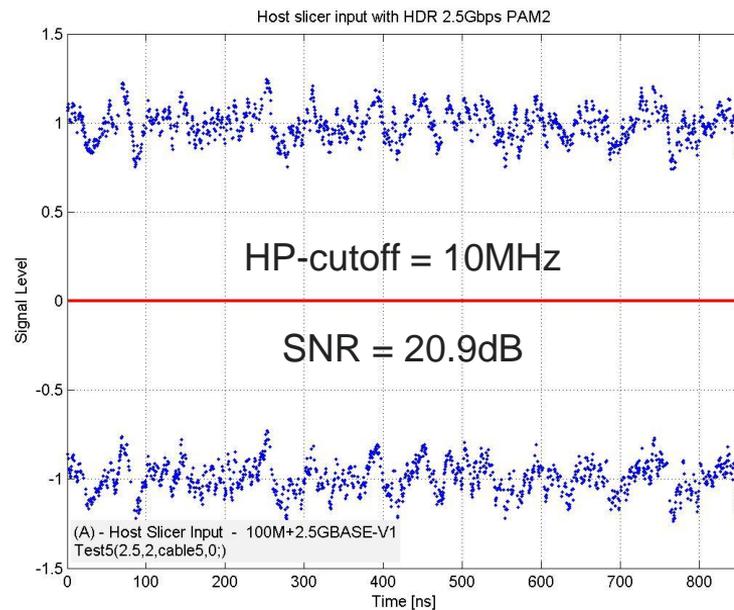
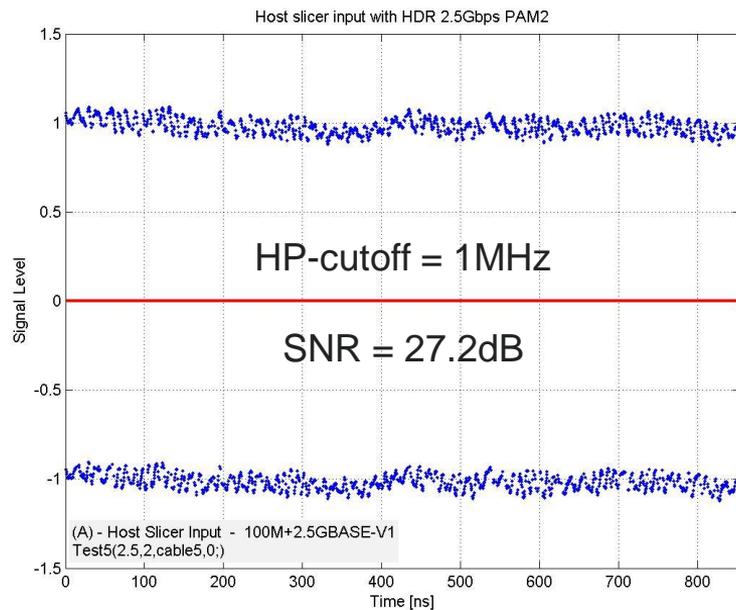
4)



HP-cutoff = 0.1MHz



The Simple PHY has Base-Line Wander

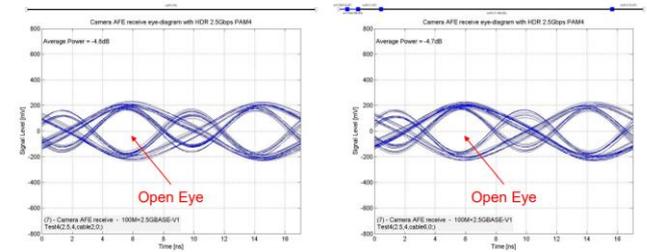


The performance impact of HP-cutoff (due to PoC) is bigger than the performance impact of echo

Simple Low Data Rate Receiver

- The ACT/GMSLE low data rate receiver is significantly simpler than even the simple high data rate receiver
- Both simulations and measurements taken from ACT-based PHY silicon confirm that no equalization is needed for the low data rate receiver
- The line rate is 24 times lower than the line rate for 2.5Gbps, which also leads to significant savings in the digital implementation
- The RS(50,46,6) FEC is also simpler than the high data rate FEC (and the proposed TDD FEC)

LDR Eye for Low and High Echo Cables



From page 6 of [jonsson 3dm 02 03 10 25](#)

Simulation of Equalizer and Echo Cancellation

- **No echo cancellation** is used for either high or low data rate signals
- **No equalization** is used for the 100Mbps DME signal
- T/2-spaced equalizers are used for the high data rate signals, to minimize ambiguity due to sampling phase at the ADC
- The equalizer has 30 FFR taps and 10 DFE taps
- Equalizer coefficients for high data rate signals are calculated using line probing signals and closed form minimum mean square equalizer algorithm from [1]
 - The noise estimate is set to zero, so this becomes zero-forcing equalizer solution

[1] R. H. Jonsson, "DSL Channel Equalization" in *Fundamentals of DSL Technology* P. Golden, H. Dedieu, and K. S. Jacobsen, Eds. CRC Press, 2005, pp. 299-350.

From page 5 of [jonsson 3dm 01b 01 20 25](#)

Summary

- The simple equalization structure suggested for TDD in [Chini_3dm_02b_0325.pdf](#) is equally applicable to ACT/GMSLE
- It was shown that Base-Line Wander (BLW) can be a bigger problem than residual echo
 - The BLW problem will impact both ACT/GMSLE and TDD
- The low data rate receiver is much simpler than the “simple” high data rate receiver
- Both simulations and measurements taken from ACT-based PHY silicon confirm that no equalization is needed for the low data rate receiver
- Both simulations and measurements taken from ACT-based PHY silicon confirm that no echo cancelation is needed for either low data rate or high data rate ACT receivers



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