Evolution of 100G Host to Module

IEEE CEI-28G VSR AdHoc

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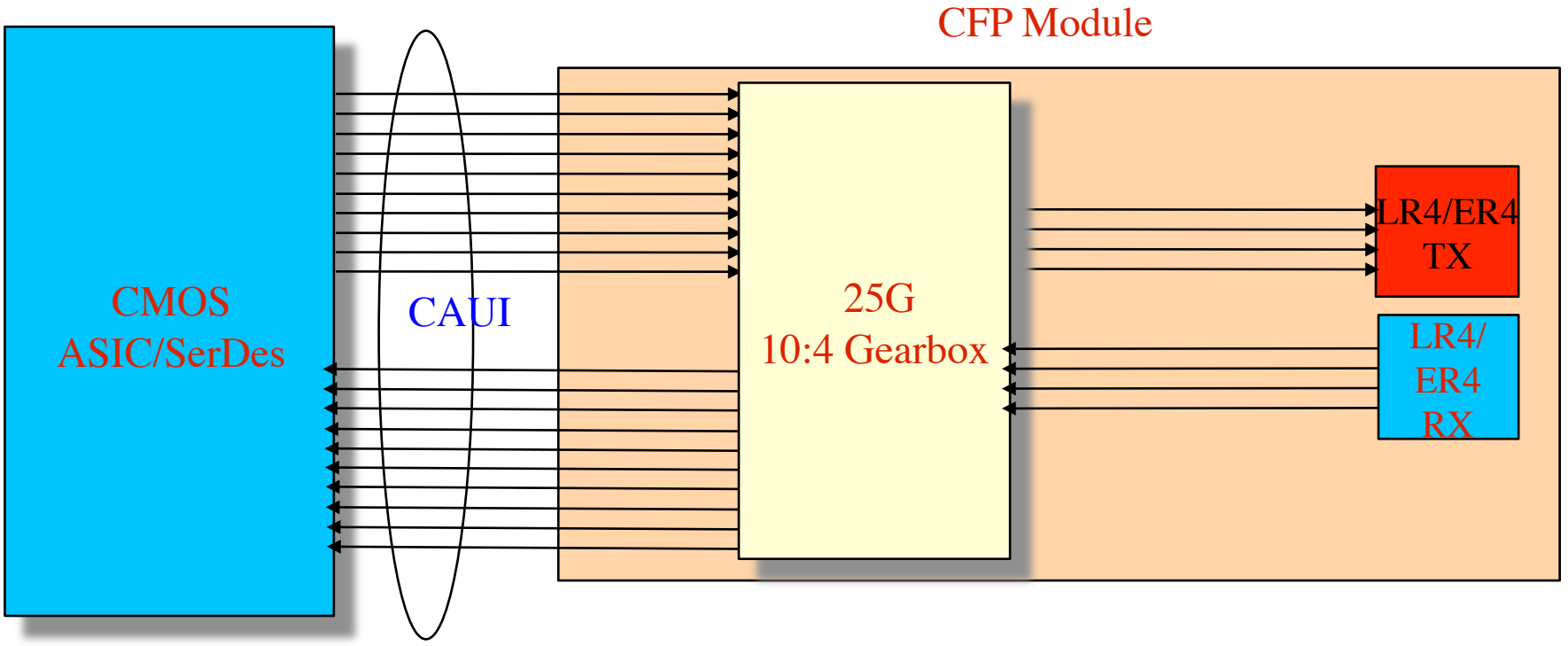
Overview

- **Short term need has given rise to VSR application model with 4" host PCB**
- **Longer term 100 GbE applications, FC, and IB need longer PCB traces 10" instead of 4"**
- **QSFP2 PD may not allow any retiming**
- **How do we make sure we don't end up with twice or 4 times as many interfaces!**

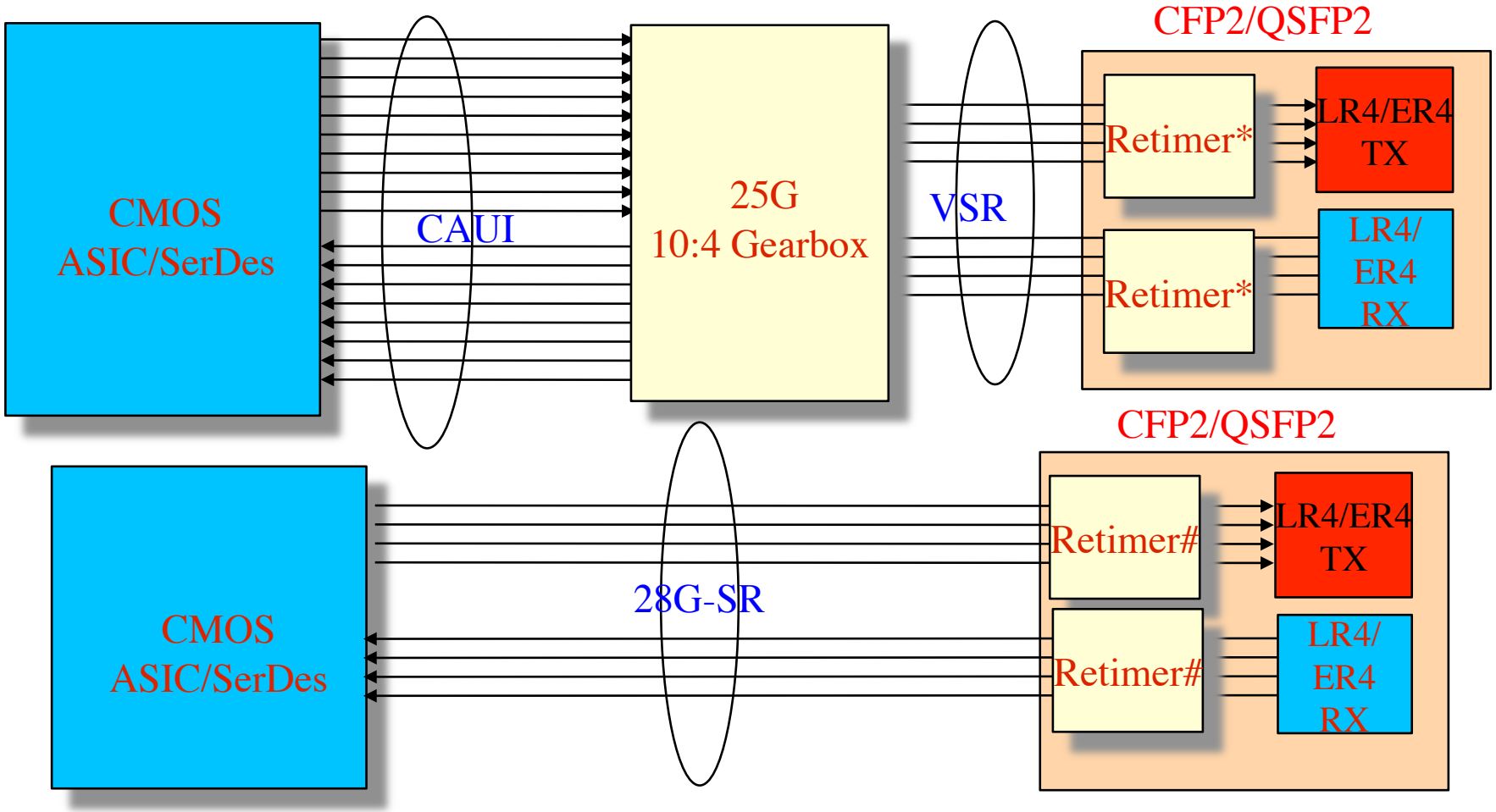
100 Gig CFP Module (Gen I) "Market Enabler"

- **Robust but too big and we all agree!**



Possible 28G Applications Model

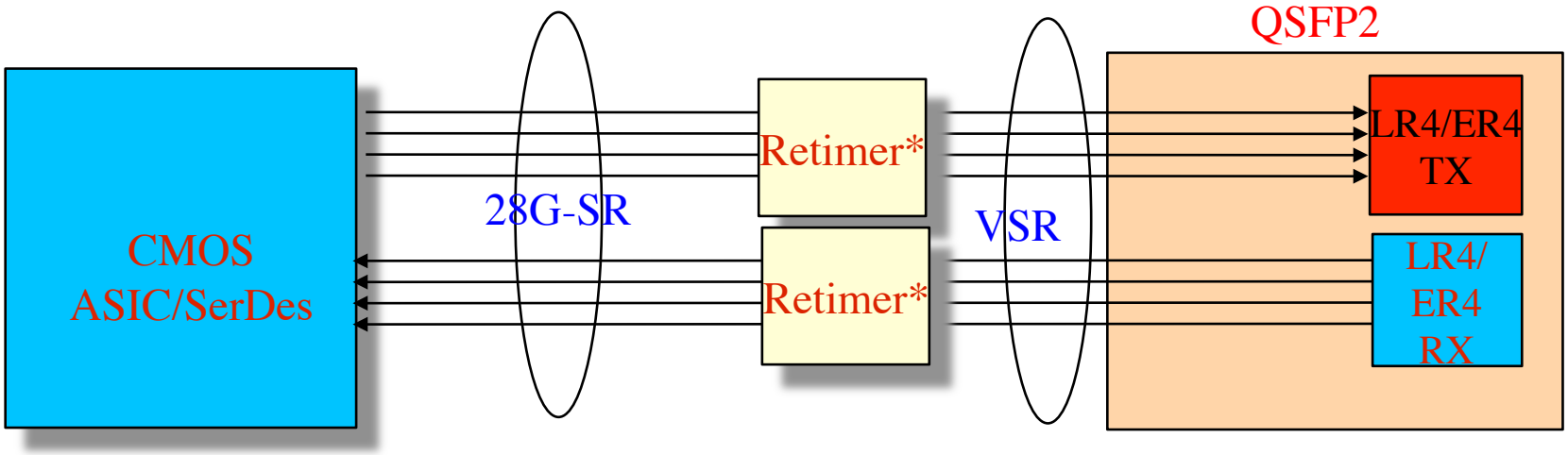
- **Application model emerging**



*Full retiming my not be required

#Full retiming likely required but PD will exceed QSFP2 limit

28G Applications Model Cont.



*Assuming in the case of QSFP2 the retimers are external it solves the power issue and distance

Option Moving Forward

- **QSFP2 likely has to be unretimed/half retimed due to PD and CFP2 could be retimed fully, option on how to proceed?**
  - **Define 4" full retime**
  - **Define 10" retime**
  - **Define unretime/half retime**
  - **Define 4" full/half retime**
  - **If we do not create a super-set then we can end up with 4 plausible interfaces!**
- **Propose to have two interfaces**
  - **Phase I- nAUI like interface to support 4" host PCB without back channel and 10" with back channel**
  - **Phase II- nPPI like interface to support 4" of host PCB**