Delay Analyze of Ethernet Passive Optical Network Over Coax

- Impacts of Duplexing Delay

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Source of Packet Delay in EPOC

Packet delay in EPON
- Propagation delay: ~ 100 us one-way for 20 km of SMF
- Physical layer and scheduling delay: about 50 us
- Total RTT : ~250 us

Packet delay in EPOC
- Additional propagation delay at coaxial cable
- Additional OFDM frame processing delay
- Additional Duplexing delay

Duplexing delay for FDD and TDD
- FDD: Duplexing delay = 0
- TDD: Duplexing delay depends on duplexing cycle time, OFDM symbol size, OFDM frame size and EPON scheduling protocol

How much delay will break the EPON protocol?

TDD Duplexing Delay

Source for TDD Duplexing Delay

- Duplexing cycle time
  - OFDM frame size
    - OFDM symbol size
      - » Cable echo delay
      - » Efficiency
- EPON scheduling and DBA
  - TDD version of EPOC is essentially a two-level scheduling system
  - There is coloration between Two schedulers

Impacts of Duplexing delay on EPOC

- Introduce extra packet delay compare with that of FDD
- Duplexing jitter - additional jitters caused by the interaction of two schedulers

Duplexing delay and jitter affects delay sensitive services and applications that require actuate timing

Large additional duplexing delay may break the EPON protocol

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TDD Duplexing Delay Analyze Model

- EPOC OLT and CNU operates in Report - Gate mode, like EPON
  - CNU send Report message during it's window cycle
  - OLT send Gate message for the next window cycle
- CNU window cycle perfectly aligns with TDD Uplink Cycle (best case for TDD)
  - This is an ideal case
  - With multiple CNUs, TDD cycle time cannot align with all window cycles
- A packet could arrives at CNU during it's window cycle and TDD Uplink cycle
- A packet could also arrives out side of TDD Uplink cycle

Fixed Upstream/Downstream ratio

- Dynamic US/DS ratio does not natively work for EPON

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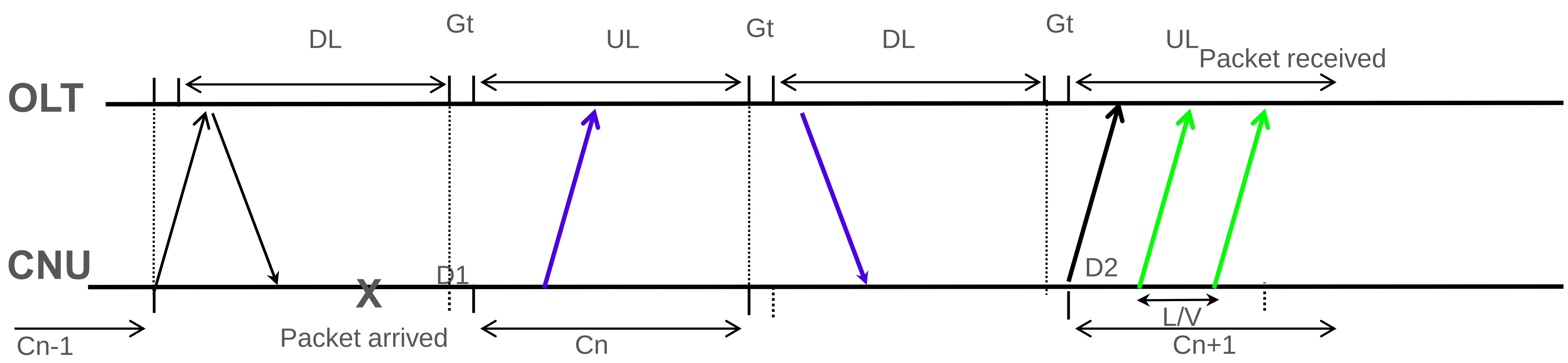
TDD Duplexing Delay Analysis (Case A)



DL: TDD Downlink cycle time

UL: TDD Uplink cycle time

Cy: TDD cycle time

Gt: TDD guard time

Cn: The nth cycle of CNU

X: Packet with length L arrived

D1: Residual cycle - the time from the instant the packet arrived to the end of DL cycle.

D2: The time CNU start n+1 cycle to the instant packet X starts to transmit

L/V: The transmission time of X

t: one way propagation delay time

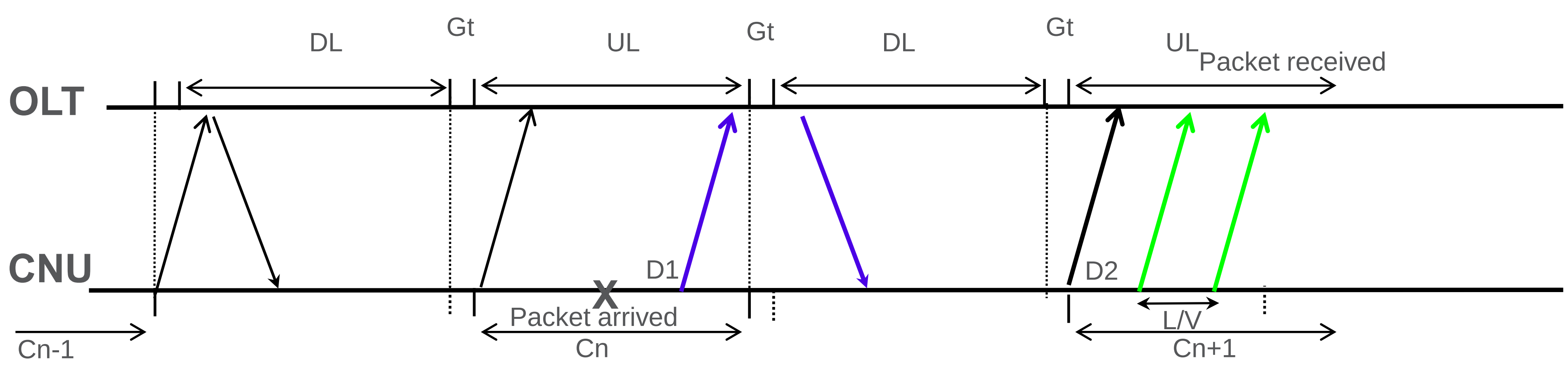
$$D = D1 + 3Gt + UL + DL + D2 + L/V + t$$

$$= D1 + 2Gt + Cy + D2 + L/V + t$$

$$= FDD + Cy + 2Gt$$

TDD Duplexing Delay Analysis (Case B)

Packet X arrives at CNU during TDD UL cycle



DL: TDD Downlink cycle time

UL: TDD Uplink cycle time

Cy: TDD cycle time

Gt: TDD guard time

Cn: The nth cycle of CNU

X: Packet with length L arrive

D1: the time from the instant the report is sent

D2: The time CNU start n+1 cycle to the instant packet X starts to transmit

L/V: The transmission time of X

t: one way propagation delay time

$$D = D1 + 2Gt + DL + D2 + L/V + t$$

$$= D1 + Gt + 0.5\ Cy + D2 + L/V + t$$

$$= FDD + 0.5\ Cy + Gt$$

EPOC Packet Delay Analysis (one way upstream)

- Upstream one way Packet delay in TDD mode = Delay in FDD mode + ((TDD cycle time Cy) or 0.5* (TDD cycle Cy))
  - Ignoring the extra Gt or 2Gt
- TDD duplexing jitter = 0.5 * Cy
- Maximum Duplexing delay for TDD mode EPOC = 2* Duplexing delay of HiNOC
- HiNOC MAP cycle time is 4096 us. Assuming 50/50 fixed DL/UL ratio:
  - Maximum Duplexing delay EPOC in TDD mode ≧ 4 ms if using HiNOC PHY
  - Duplexing jitter could be as large as 2 ms
  - Duplexing jitter alone is comparable to IFDV in MEF (≦ 3ms required in MFE 23H)
- Total delay of EPOC in TDD mode ≧ 5 ms
  - Assuming 1 ms FDD delay; TDD PHY is similar to HiNOC PHY

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EPOC PHY considerations

- EPOC PHY is yet to be defined...but under the same physics equal constraints as that of HiNOC
- Coaxial cable plant echo delay is reported between 3 us to 7us
- CP should be at least ≧ cable echo delay
- CP length places a limitation on OFDM symbol size. Assuming 1/64 ratio:
  - OFDM symbol time could be 200 us to 400 us
  - or, in order to have shorter symbol time we have to accept lower efficiency
- An OFDM frame contains multiple OFDM symbols, and an TDD cycle contains multiple OFDM frames
  - That translates into more delays and additional Duplexing delays...
- Delay is a big challenge for EPOC PHY
  - It has to be constant, otherwise consistent RTT can not be guaranteed
  - It need to balanced with efficiency
  - Additional large duplexing delay could make EPOC unfeasible

Conclusions

- TDD + EPON is a two-level scheduling system
- Calculating TDD Duplexing Delay in EPOC should take EPON scheduling & DBA into consideration
- TDD version of EPOC adds additional Cy (TDD cycle time) delay, it could be, for example, as large as or great than 4 ms
- TDD mode EPOC also adds additional 0.5*Cy duplexing jitter, it could be, for example, as large as or great than 2 ms
- Coaxial cable plant echo delay places a serious constrain on the choice of OFDM symbol size:
  - Large OFDM symbol time with longer delay
  - or, relatively small symbol size with much lower efficiency
- Delay is a big challenge for EPOC PHY
  - Any additional delay could make EPOC unfeasible
  - Any additional jitter could break MEF services

Thanks