IEEE 802.3 Ethernet Working Group
DRAFT Liaison Communication

Source:	IEEE 802.3 Working Group[1]	
To:	Stefano Ruffini	Rapporteur, ITU-T Question 13/15 stefano.ruffini@ericsson.com
	Silvana Rodrigues	Associate Rapporteur, ITU-T Question 13/15 silvana.rodrigues@idt.com
	Hiroshi Ota	ITU-T SG15 Advisor tsbsg15@itu.int
CC:	Konstantinos Karachalios	Secretary, IEEE-SA Standards Board Secretary, IEEE-SA Board of Governors sasecretary@ieee.org
	Paul Nikolich	Chair, IEEE 802 LMSC p.nikolich@ieee.org
	Adam Healey	Vice-chair, IEEE 802.3 Ethernet Working Group adam.healey@broadcom.com
	Pete Anslow	Secretary, IEEE 802.3 Ethernet Working Group panslow@ciena.com
From:	David Law	Chair, IEEE 802.3 Ethernet Working Group dlaw@hpe.com
Subject:	Liaison reply to Impact on timing performance due to Ethernet PHY – October 2017 communication	
Approval:	To be approved at IEEE 802.3 Interim meeting, Geneva, Switzerland, 25th January 2018	

Dear Mr. Ruffini,

Thank you for your liaison letter concerning the impact on timing performance due to the Ethernet PHY.

We recognize the importance of controlling delay asymmetry and variability for time synchronization. To that end, Clause 90 of IEEE Std 802.3-2015 deals with methods for reporting the minimum and maximum values of transmitter and receiver path data delays separately.

Following your liaison letter, an ad hoc sub-group was formed to address the concerns that were raised and recommend further action. The outcome of this activity is reported below.

[1] This document solely represents the views of the IEEE 802.3 Working Group, and does not necessarily represent a position of the IEEE, the IEEE Standards Association, or IEEE 802.

As noted in your letter, FEC encoding includes periodic insertion of parity blocks, which creates variability in the delay of frames in the transmitter and in the receiver. This is characteristic of multiple FEC schemes specified in IEEE Std 802.3-2015 and its amendments, including Clause 108. For the RS(528,514) used in Clause 108, the delay variability is up to 5.43 ns in both transmitter and receiver. However, in all Ethernet FEC schemes, the bit streams at the encoder input and at the decoder output are identical (up to possible errors) and therefore they must be synchronous, as illustrated in Figure 1. This synchronous operation means that the delay variation in the transmit path due to transcoding is matched by an opposite delay variation in the receive path due to reverse transcoding, yielding a constant total delay, as shown in Figure 2.

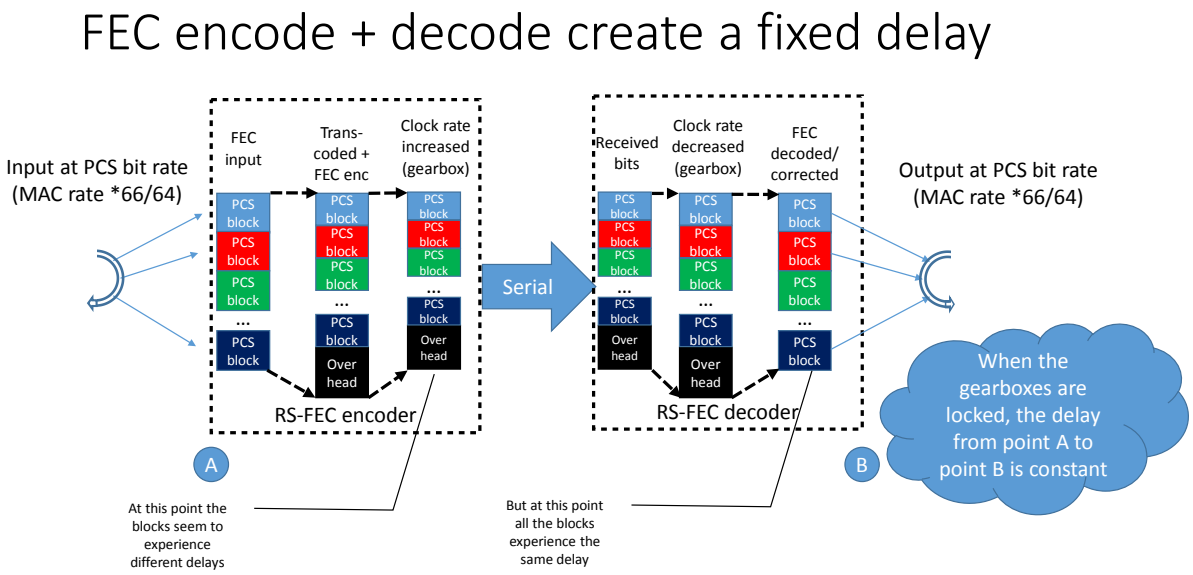

Figure 1: Synchronous FEC encoding and decoding

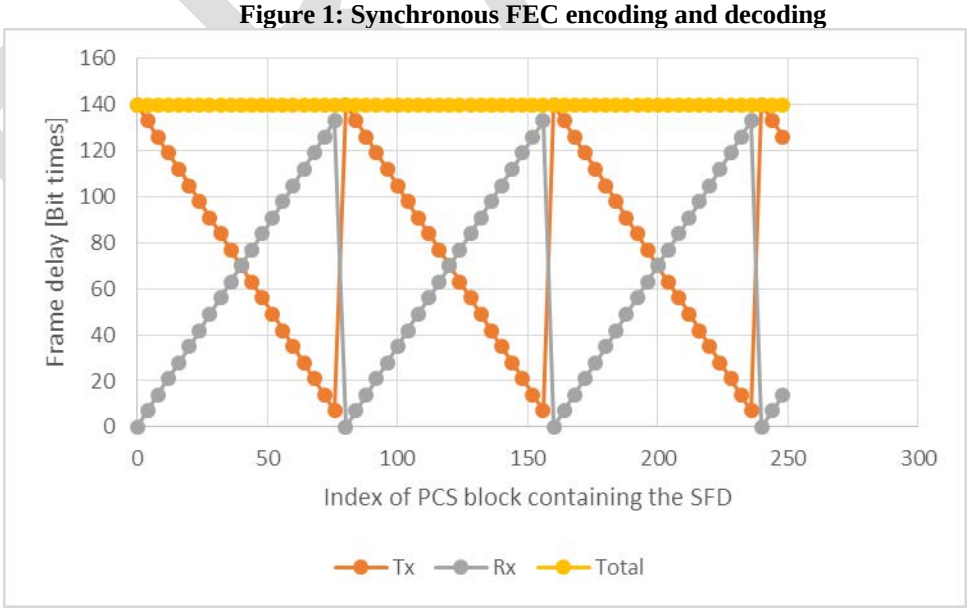

Figure 2: Frame delay due to transcoding in RS(528,514)

The fact that the delay variations cancel out is not currently addressed by Clause 90, and measurement of the path data delays in a specific device may result in a difference between the reported minimum and maximum delays in both transmit and receive data paths, which

is indistinguishable from measurement inaccuracy. To address that, a comment has been submitted to the IEEE P802.3 (IEEE 802.3cj) Revision task force, suggesting a recommendation of a specific path data delay reporting method that would eliminate this source of variability. Please note that the IEEE P802.3 (IEEE 802.3cj) Revision is currently in Sponsor Ballot and comments may or may not be accepted.

Another possible source of delay variability is the periodic insertion and deletion of markers by the PCS/FEC (e.g., codeword markers in Clause 108, or alignment markers in Clause 82). This functionality may introduce delay variability of up to 12.8 ns for the 100GBASE-R PCS, in both transmitter and receiver. However, we would like to note that there are compliant implementation methods that create no timestamping inaccuracy due to markers.

The letter also listed rate adaptation as a possible concern. Note that rate adaptation is specified as a function of the Reconciliation Sublayer (RS), and implementation within the RS does not affect timing at the xMII reference point. While some PCS specifications include optional capability of rate adaptation, implementations are possible without this capability, if minimizing delay variability is a goal.

The reference points of path data delay reporting are specified in Clause 90 as the xMII and the MDI. This enables assessment of the delays from MDI to MDI even with asymmetry in PHY delays. Since the xMII is the only reference point that is defined for all PHYs, it is the only point that enables a generic definition of delays. As noted above, accurate timing is achievable in practice, even with the marker insertion functionality, and with the proposed specification of path data delay reporting with FEC. Therefore, changing the reference point for path data delay reporting is not considered necessary.

We would like to note that the Ethernet standard does not enforce limits on delay variations in Ethernet PHYs, nor does it dictate specific implementation methods. We would also note that it may not be possible to eliminate all timing errors when certain optional internal interfaces are physically instantiated (e.g., XGXS/XAUI or 25GAUI). Products may or may not be optimized for minimum delay variation.

In summary, the action following your letter is a proposed recommendation for specific path data delay reporting that would eliminate variability due to FEC encoding and decoding, which will be processed in the IEEE P802.3 (IEEE 802.3cj) Revision task force. We would like to thank you for bringing forward your concerns. We look forward to continuing our cooperation with ITU-T SG15.

Sincerely,

David Law

Chair, IEEE 802.3 Ethernet Working Group