

IEEE 802.3  
Interpretations Report

July 24th, 2003  
San Francisco, CA  
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# Activities this week

- Met Wednesday afternoon
- 2 Interpretations considered
  - 1-07/03 - Globally assigned multicast address bit order
  - 2-07/03 - XGXS align status register bits

**Interpretation Number:** 1-07/03 (Globally assigned multicast address)  
**Topic:** Globally assigned multicast address bit order  
**Relevant Clause:** Annex 31B  
**Classification:**

### **Interpretation Request**

Standard: IEEE Std 802.3-2002.

I should need a clarification/interpretation about the standard IEEE 802.3.

Consider the Annex 31B (MAC Control PAUSE operation) of the standard IEEE Std 802.3-2002 (pag. 571).

With reference to the globally assigned 48 bit multicast address

01-80-C2-00-00-01,

it's not clear which is the right order of nibble transmission on the MII interface.

There are 2 possible orders of transmission of the nibbles on the MII interface:

a) 1-0-0-0-0-0-2-C-0-8-1-0

In this case, I'm supposing the first octet of the address is the high order byte.

b) 1-0-0-8-2-C-0-0-0-0-1-0

In this case, I'm supposing the first octet of the address is the low order byte.

## Annex 31B

(normative)

### MAC Control PAUSE operation

#### 31B.1 PAUSE description

The PAUSE operation is used to inhibit transmission of data frames for a specified period of time. A MAC Control client wishing to inhibit transmission of data frames from another station on the network generates a MA\_CONTROL.request primitive specifying:

- a) The globally assigned 48-bit multicast address 01-80-C2-00-00-01,
- b) The PAUSE opcode,
- c) A request\_operand indicating the length of time for which it wishes to inhibit data frame transmission. (See 31B.2.)

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames.

PAUSE frames shall only be sent by DTEs configured to the full duplex mode of operation.

The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been reserved for use in MAC Control PAUSE frames for inhibiting transmission of data frames from a DTE in a full duplex mode IEEE 802.3 LAN. IEEE 802.1D-conformant bridges will not forward frames sent to this multicast destination address, regardless of the state of the bridge's ports, or whether or not the bridge implements the MAC Control sub-layer. To allow generic full duplex flow control, stations implementing the PAUSE operation shall instruct the MAC (e.g., through layer management) to enable reception of frames with destination address equal to this multicast address.

### 3.2.3.1 Address designation

A MAC sublayer address is one of two types:

- a) *Individual Address*. The address associated with a particular station on the network.
- b) *Group Address*. A multdestination address, associated with one or more stations on a given network. There are two kinds of multicast address:
  - 1) *Multicast-Group Address*. An address associated by higher-level convention with a group of logically related stations.
  - 2) *Broadcast Address*. A distinguished, predefined multicast address that always denotes the set of all stations on a given LAN.

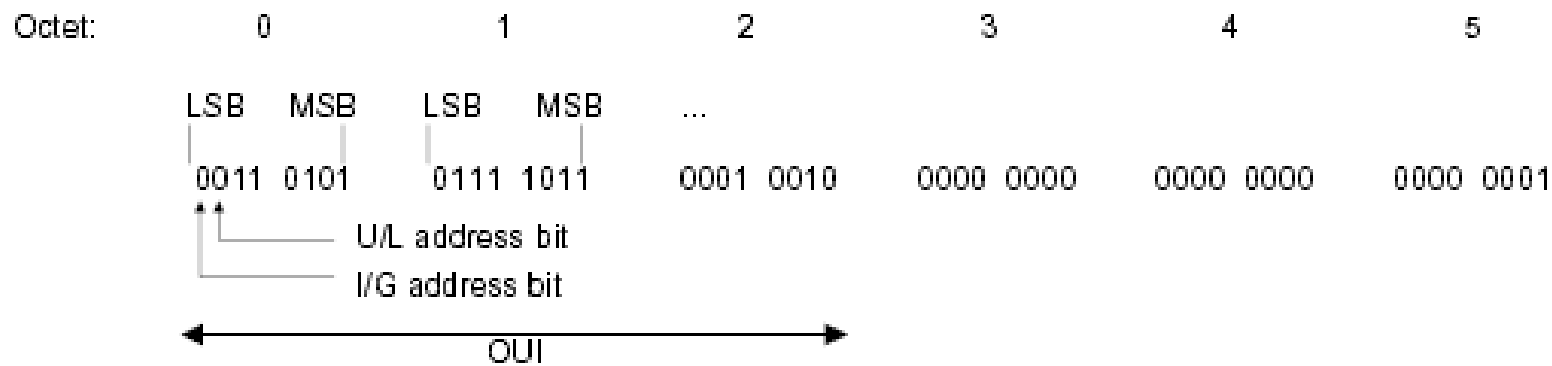
All 1's in the Destination Address field shall be predefined to be the Broadcast Address. This group shall be predefined for each communication medium to consist of all stations actively connected to that medium; it shall be used to broadcast to all the active stations on that medium. All stations shall be able to recognize the Broadcast Address. It is not necessary that a station be capable of generating the Broadcast Address.

The address space shall also be partitioned into locally administered and globally administered addresses. The nature of a body and the procedures by which it administers these global (U) addresses is beyond the scope of this standard.<sup>12</sup>

<sup>12</sup>For information on how to use MAC addresses, see IEEE Std 802-2001, Overview and Architecture. To apply for an Organizationally Unique Identifier for building a MAC address, contact the Registration Authority, IEEE Standards Department, P.O. Box 1331, 445 Hoes Lane, Piscataway, NJ 08855-1331, USA; +1 732 562 3813; fax +1 732 562 1571. URL: <http://standards.ieee.org/>.

<sup>13</sup>Type field assignments are administered by the Registration Authority, IEEE Standards Department (see Footnote 12 for address).

Hexadecimal representation: AC-DE-48-00-00-80  
 Bit-reversed representation: 35:7B:12:00:00:01



Octet 0	1	0	1	0	1	1	0	0	U/L address bit
Octet 1	1	1	0	1	1	1	1	0	I/G address bit
Octet 2	0	1	0	0	1	0	0	0	
Octet 3	0	0	0	0	0	0	0	0	
Octet 4	0	0	0	0	0	0	0	0	
Octet 5	1	0	0	0	0	0	0	0	

Figure 8—Universal address

# 1-07/03 Proposed response

IEEE Std 802.3 clearly references the required information in subclause 3.2.3.1 'Address designation' which includes a footnote attached to the last paragraph which states 'For information on how to use MAC addresses, see IEEE Std 802-2001, Overview and Architecture.'

Referring to IEEE Std 802-2001, subclause 9.2, '48-bit universal MAC addresses', the third paragraph of subclause 9.2.1 'concept' states:

The standard representation of a 48-bit LAN MAC address is as a string of six octets, using the hexadecimal representation (3.1.8). In certain contexts associated with use of IEEE 802.5 frame formats, LAN MAC addresses may be represented using the alternative bit-reversed representation (3.1.2). See 9.5 for further specification relating to use of the bit-reversed representation.

NOTE - The upper, bit-stream representation of the universal address in Figure 8 shows the LSB of each octet first; this corresponds to the data-communications convention for representing bit-serial transmission in left-to-right order, applied to the model for transmission of LAN MAC address fields (see 6.2.3). See also 9.5 for further discussion of bit-ordering issues. The lower, octet-sequence representation shows the bits within each octet in the usual order for binary numerals; the order of octet transmission is from the top downward.

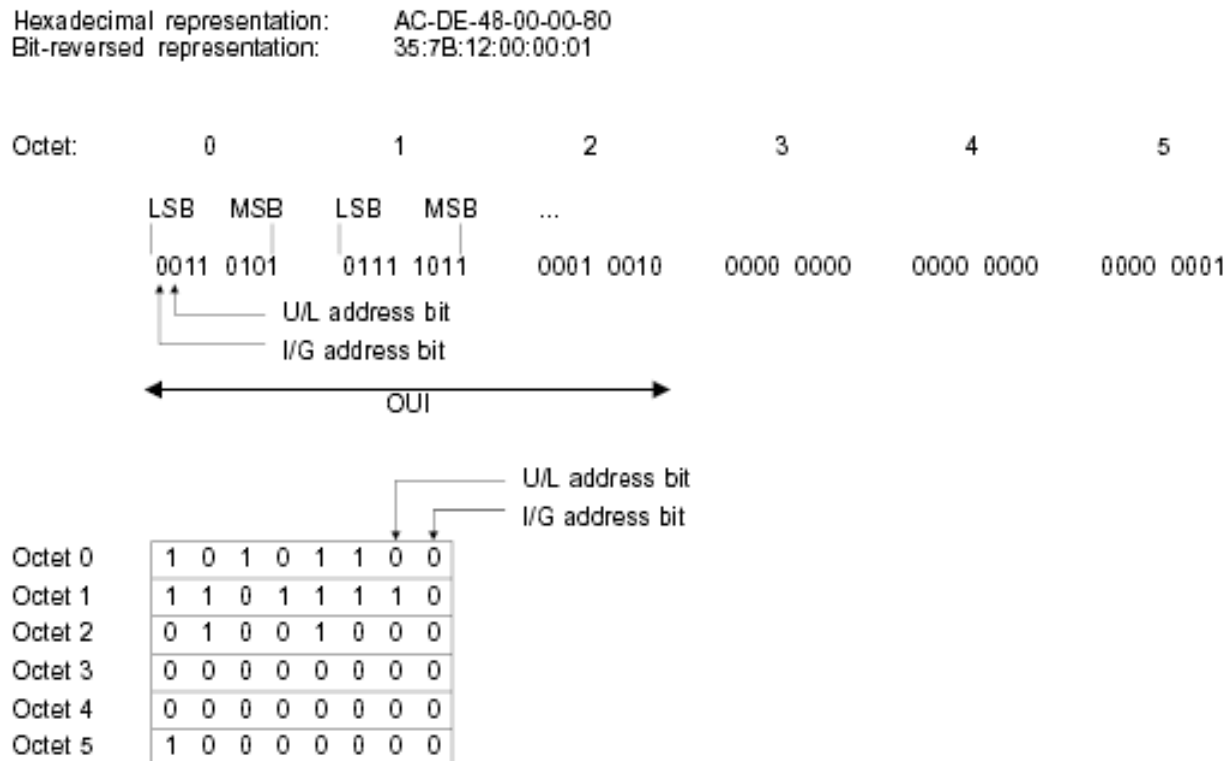


Figure 8—Universal address



# 1-07/03 Proposed response (cont)

This provides a clear mapping from the address written out in the standard and its transmission order.

Due to the infrequency with which the hexadecimal address format appears within 802.3 it may not be obvious that Clause 3 contains the needed reference. Due to this we will submit a maintenance request that will propose to add a cross reference back to subclause 3.2.3.1 from Annex 31B.

In addition Figure 22-11 in subclause 22.2.3 provides additional information on the bit and nibble transmission order across the MII.

Classification: Unambiguous

# Interpretation request 2-07/03

1. Related Standard: IEEE Std 802.3ae-2002, clause 45.2.4 and clause 48

It appears that there seems to be a contradiction in the control bit description when using the terms “receive” and “transmit” in clause 45 and clause 48.

In general, clause 48 refers to “transmit” as the direction in which data is sent to XAUI, while “receive” is the direction in which incoming data from XAUI is accepted, synchronized and deskewed. This is clearly stated in Figure 48-2. Additionally, Table 48-7 assigns the state “align\_status” to the Management Register Bit “4.8.10 Receive local fault”.

In subclause 45.2.4.8.1, the definition of register bit “4.24.12 PHY XGXS lane alignment status” describes this bit as “PHY XGXS transmit lane alignment status”. This is a contradiction to the definition given in clause 48. It should better read “PHY XGXS receive lane alignment status”, because lane alignment is only done in receive direction and there is no data alignment in transmit direction. Consequently, bit 4.1.2 should be renamed because it is the latched status of bit 4.24.12.

We suggest to change the text in clause 45 to read as:

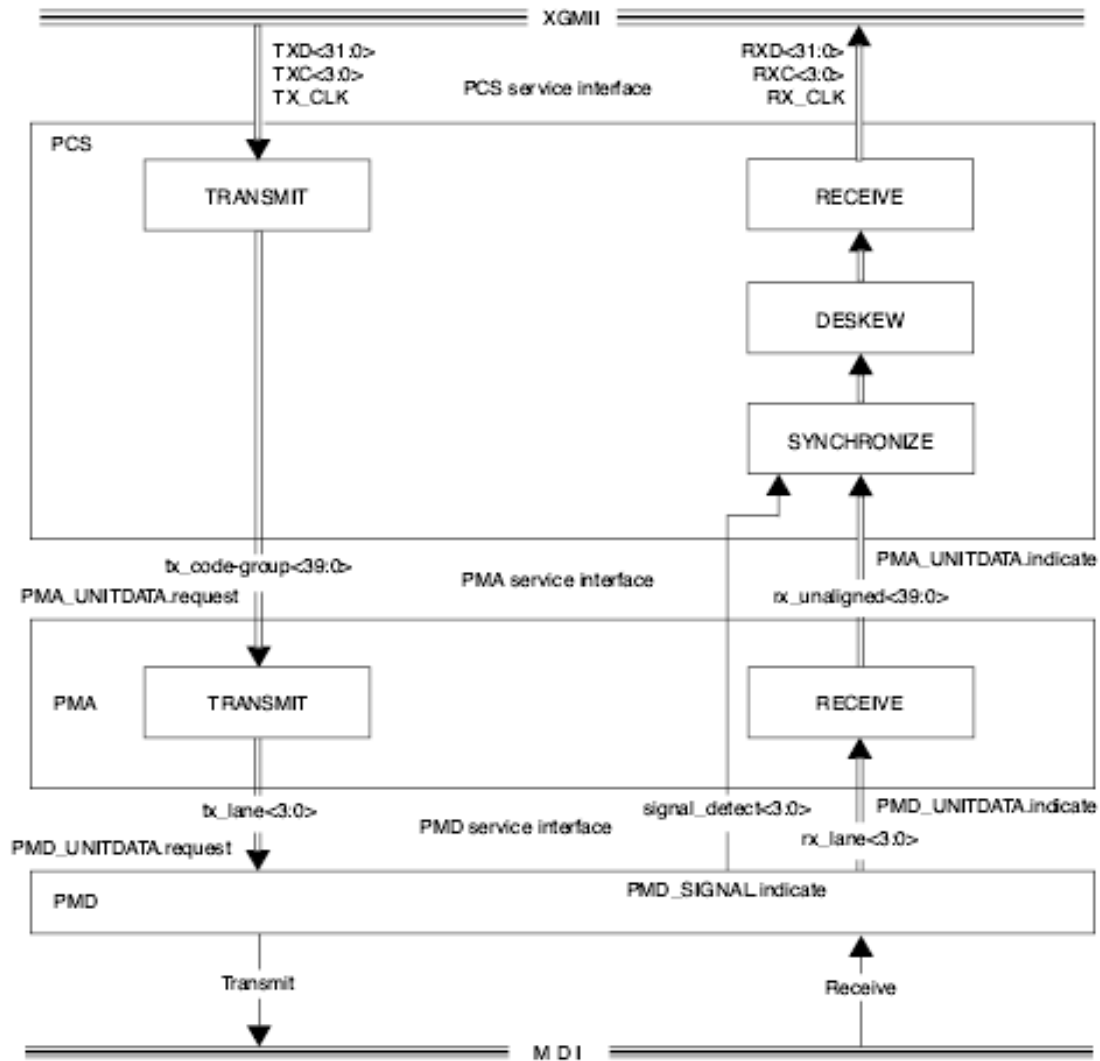
#### **45.2.4.2.2 PHY XS receive link status (4.1.2)**

When read as a one, bit 4.1.2 indicates that the PHY XS receive link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS receive link is not aligned. The receive link status bit shall be implemented with latching low behavior.

#### **45.2.4.8.1 PHY XGXS receive lane alignment status (4.24.12)**

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four receive lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four receive lanes.

...

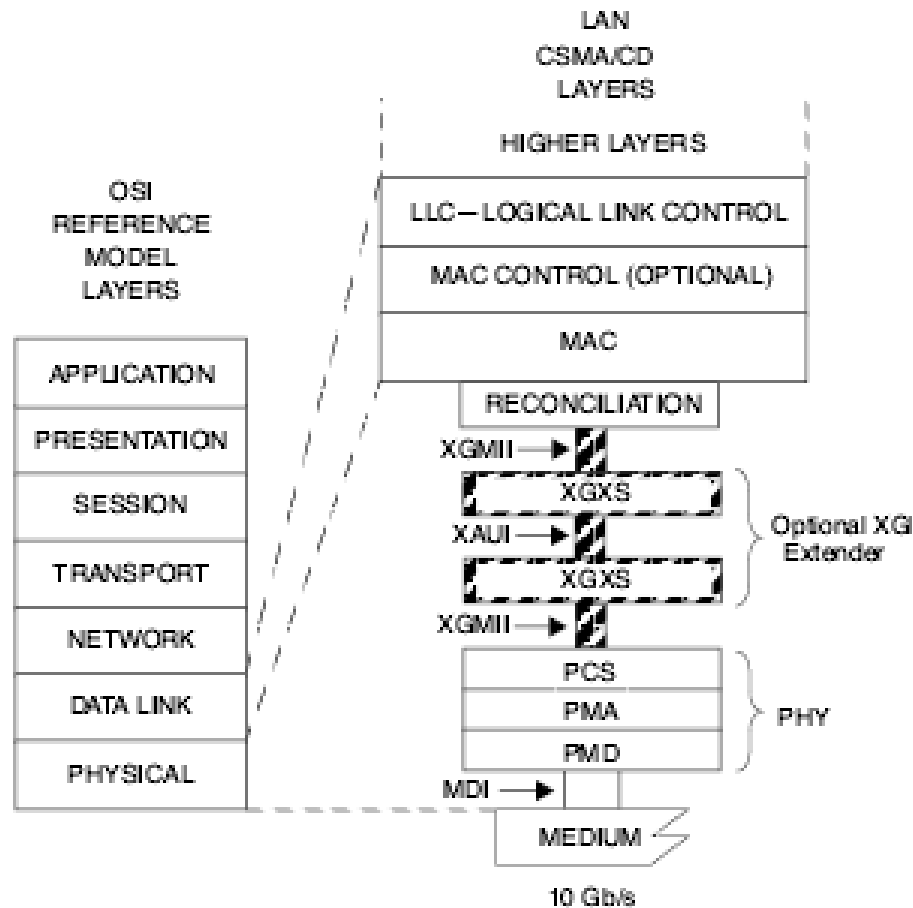


**Figure 48-2—Functional block diagram**

### 48.1.7 Functional block diagram

Figure 48-2 provides a functional block diagram of the 10GBASE-X PHY.

# 47. XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)



## 47.2.1 PCS and PMA functionality

The XGXS shall meet all mandatory portions of 48.2 and 48.3, and may meet any optional portions of 48.2 and 48.3. Since the PHY XGXS operates with the XGMII below the XAUI, the transmit requirements of 48.2 and 48.3 apply to the PHY XGXS receive requirements and the receive requirements apply to the PHY XGXS transmit functionality.

# 2-07/03 Proposed response

Clause 48 specifies the 10GBASE-X PMA and PCS and does not specify XAUI which, while built upon the 10GBASE-X PMA and PCS specification, is specified in Clause 47. In particular Figure 48-2 illustrates a 10GBASE-X PHY as stated in subclause 48.1.7, and not XAUI.

Within the Clause 47 XAUI specification, subclause 47.2.1 states 'Since the PHY XGXS operates with the XGMII below the XAUI, the transmit requirements of 48.2 and 48.3 apply to the PHY XGXS receive requirements and the receive requirements apply to the PHY XGXS transmit functionality.' As an example of this the PHY XGXS transmit function includes a lane alignment and therefore a PHY XGXS transmit lane alignment status bit is provided in subclause 45.2.4.8.1.

Based on this reversal defined in subclause 47.2.1 the bit definitions related to the PHY XGXS in Clause 45 are correct.

Classification: Unambiguous

# IEEE 802.3 Motion

IEEE 802.3 approves the proposed Interpretation responses to the Interpretation requests 1-07/03 and 2-07/03 as presented without the need for a 30 day letter ballot.

M: David Law

S: Steve Carlson Tech 75%/Proc ~~50%~~

~~PASSED/FAILED~~

Date:24-Jul-2003

Y: 77

N: 0

A: 0

Time: 2:46PM